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TIG501, Tiny Tiger controller board for small embedded control applications.

The BASIC Tiger and Tiny Tiger microprocessor modules from Wilke (Ger many) pres ent an easy way for builders of embedded control systems to build, program and put small systems into production. The modules are available in a range of memory capacities: Tiny Tigers can have 128kB/32kB, 128kB/128kB, 512kB/512kB or 2MB/512kB respectively of FLASH and RAM.

This board uses theTiny Ti ger mod ule and places it on an 116mm by 101mm board to make it easy for sci en tists and engineers to use the Tiny Tiger for small systems without having to design a printed circuit board. The board has a Xilinx XC5202 gate array and input protection or FET drivers between the Tiger and all the I/O screw terminals, isolating the Tiger from the outside world for ESD and EMC purposes. Tiger pins are bypassed to a grounded PCB plane, and all sup ply rails and Tiger pins are EMC filtered.

(JED also makes a larger Tiny Tiger board, the TIG505, for users who need more I/O, larger gate array, larger key boards and ex tra in ter faces.)

The Xilinx can be reprogrammed by users downloading a data file from the FLASH, so users can re-wire the system be tween the pins and the Ti ger, add ing their own counters, pulse gen era tors, shift- register fil ters, etc.

Users of this board have 12 digital input terminals, 4 ana log in put terminals, 13 out puts with open- drain FETs, and a swit ched 5 volt out put. There are two se rial ports for communication. One of these ports can by used with an optional opto- isolated RS485 in ter face.

This board can be used as a con ven tional single- board- computer, or can have a 4- line by 20 char ac ter LCD added on top, with a five- key set of push- buttons (or a small XY key board) for "menu" style op era tor set ups, etc.

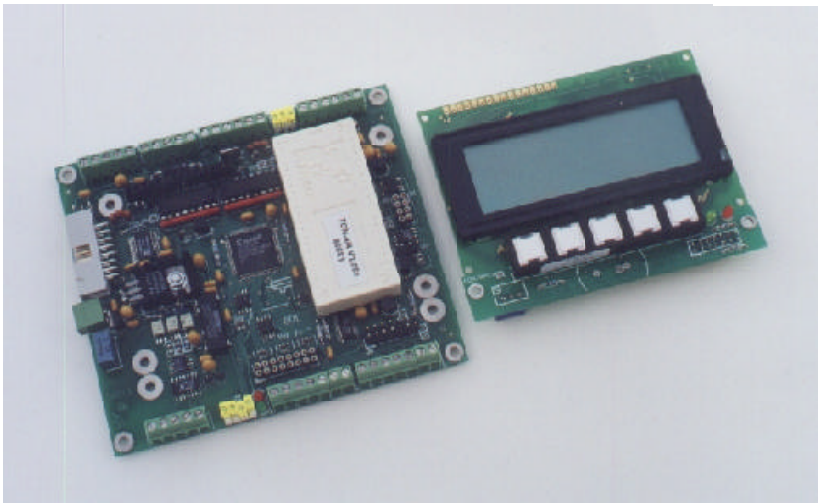
The Tiger concept and EMC.

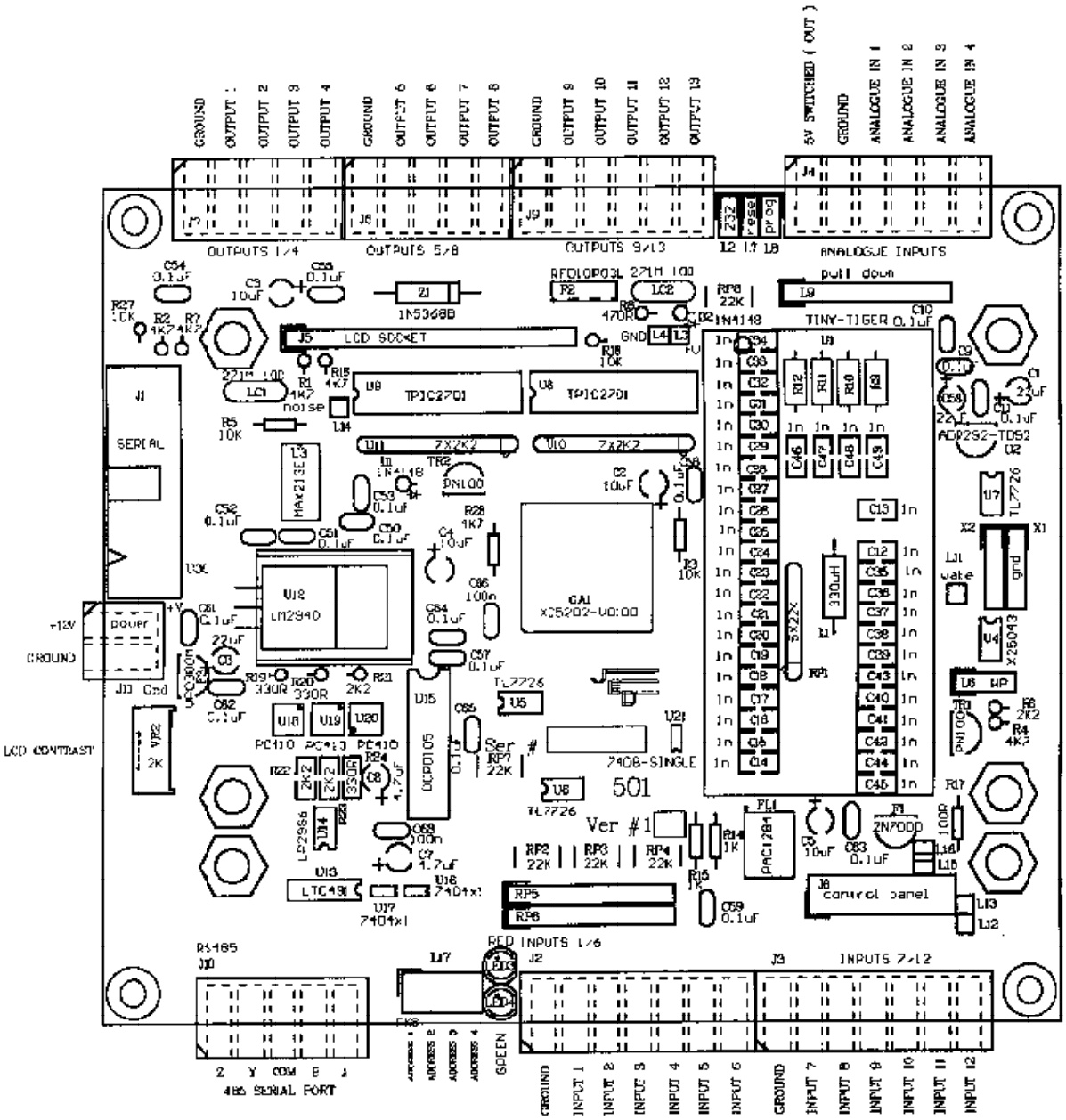
The BASIC and Tiny Tigers are small, 20 Mhz clock microprocessor modules with the high speed bus and mem ory sys tem housed in a plastic housing, ready to use in applications with out us ers hav ing to worry about the in tri cacies of high speed bus tim ing, de cod ing or pag ing and ad dress ing. The in ter faces nec es sary for a standard small microprocessor system, (dual UARTs, a complex counter-timer system, plenty of mem ory (FLASH and CMOS, battery- backed RAM), Real- Time- Clock and a ten- bit four channel analog input system) are all housed in the module.

AUSTRALIAN MADE

(May 1999)

- Uses Tiny Tiger from Wilke Technology (Germany), and allows high-performance systems to be developed at low cost, direct from a PC;
- Low power: board draws approx. 100 mA;
- BASIC multitasking allows modular development of programs with controlled interaction between segments. (Up to 32 tasks allowed);
- Powerful development system runs under Windows, edits, downloads to FLASH and remotely debugs target at source level;
- JED board made in Australia to support the Tiger allows "screwdriver" building of systems, with gate-array reprogramability of hardware in a Xilinx gate array;
- Xilinx provides Dallas iButton support via hardware timing generator; and
- Opto-isolated RS485 interface for local area serial networking (optional).





Because all the high-speed bus ses oc cupy a small volume, RF radiation is very much reduced over a system where the bus ses oc cupy a large PCB sur face area act ing as an an tenna. All I/O lines from the Ti ger are by passed to the ground plane on the back of this board, so any RF which es capes via de vice pins is by passed bef ore it can radiate. Supply lines are also L-C filtered.

Memory system and download mode.

The TIG501 board can have a choice of any of the four different Tiny Tigers installed, with RAM from 32kB to 512kB and FLASH from 128kB to 2 MB.

The choice ob vi ously de pends on pro gram size, but users should be aware that if an LCD display is used, the complex device drivers pro vided only al low about 10 kB of RAM for user data, and so most ap pli ca tions, ex cept for very price-sensitive proj ects, would be well ad vised to use at least the TCN-1/1 (128kB/128kB).

Download to the FLASH occurs when the compiler pro gram (run ning on the PC con nected to a se rial port) detects a download request. The Tiger must have the PC jumper switch set to "PC mode" as RE SET is trig gered.

Xilinx gate array and options it provides.

A Xil inx XC5202 gate ar ray in a 100 pin pack age provides the TIG501 sys tem with 81 I/O lines and 64 Con figu rable Logic Blocks, (with four flip-flops and function gen era tors each). It is a low-power, RAM-based gate array, so af ter power-up or re set it is nec es sary for the Ti ger to run a small program to load the con figu ra tion bit map into the Xilinx. The file is loaded into the FLASH by a DATA state ment in the pro gram at com pile time, and the Xilinx loader program reads it from there and loads the Xil inx. (This takes about a sec ond).

There is suf fi cient space in this de vice for quite a lot of logic: it can be de signed on a screen us ing sche matic en try soft ware and routed us ing the Foun da tion low-cost de velopment package from Xilinx. The advantage of such a

con fig ur able hard ware sys tem is the one PCB and I/O system can have its hardware completely redesigned or altered in quite sim ple ways. Also, once the board or con trol sys tem has been tested for EMC with a worst- case de sign, al tera tions in the gate ar ray need no re cer ti fi ca tion.

Input system, on 14 screw terminals.

Across the top of the lower edge of the TIG501 board are twelve general-purpose input connectors (and two ground screw terminals). Input lines can be pulled up to Vcc or down to ground with a re sis tor ar ray, usu ally 4k7. A se ries re sis tor con nects the in put pin to the gate ar ray, with a 7726 ac tive clamp on the line to Vcc and Ground, so that the gate ar ray is not dam aged by ex cess volt ages or electrostatic pulses to the pin. Input voltage ranges can range + to - 24 volts con tinu ously but can with stand much larger ESD tran sients. The thresh old is at TTL lev els.

This in put ar range ment al lows us ers to se lect be tween a voltage input mode (pull-down resistor to ground), or contact or opto-isolator mode (pullup re sis tor to Vcc).

The standard JED gate array provides these inputs to read able ports im ple mented in the gate ar ray at ad dresses 80 and 81 (hex).

Considerable power is provided in the Xilinx gate array. Many flip-flops are available to build logic between the input pins and the registers read by the Tiger IN instruction.

The PLSOUT instruction in the Tiger (Port P86) is routed on the board to a global clock on the Xil inx, and so can be used to gen er ate time bases for coun ters and tim ers im ple mented in the gate ar ray. This is pro gram ma ble over a wide range of fre quen cies: typi cally it is set to 500 kHz.

Output ports, on 17 screw terminals.

The out puts con sist of 13 N- channel power FETs with the sources grounded and the drains con nected to the ter mi nals. Each out put has a fly wheel catch- diode to a zener to 47 volts. The driv ers are TPIC2701s, with a pull- down resistor on the gate of each FET to en sure it is OFF with the gate ar ray un ini tal ised on RE SET.

A 14th output is a P- channel power-FET with drain to Vcc, pro vid ing a switched 5 volt rail out put (to power sensors, etc.)

The stan dard gate ar ray al lows the FETs to be driven 8-bits in parallel, at addresses 10 and 11 (hex) using the OUT in struc tions, which in clude masks al low ing in di vid ual bits or groups of bits to be ad dressed with out af fect ing others in the same port. Users can add their own driving logic in the Xil inx gate ar ray. This can in clude coun ter and pulse gen era tion logic, to, for ex am ple, drive step per motors.

Serial ports, RS232 and (optional) RS485.

A 16- pin con nec tor at the left- hand side of the TIG501 has its first 9 pins allocated for SERIAL-0 RS232 port, wired as a DE (i.e. the same as a PC would pig nut to a D9 connector.) A null-modem cable is necessary to connect this port to a PC, but it can con nect to a mo dem (D9 or D25 via an adaptor) directly. The Tiger supports CTS/RTS handshake with the SERIAL-0 driver, but the other RS232 lines ter mi nate in ports in the Xil inx and are read able or set ta ble by IN or OUT in struc tions.

SERIAL-1 RS232 has three wires (TX, RX and Gnd) on the same connector, and this connects to the PC for down load. Down load mode from the PC is se lected by the PC/RUN switch.

An op tional RS485 full du plex (4- wire) or half- duplex (2- wire) can be factory- installed on the TIG501 if it is intended to use the board in multi-drop distributed RS485 net works. The in ter face is fully opto- isolated, and the TX "connect- to- line" func tion is pro vided in the Xil inx with a hardware timer.

A 5-pin screw terminal connects to the RS485 lines. Switchable ter mi na tions are avail able on both RX and TX lines, and bi asing re sis tors are pro vided on the RX line as well (when the RX termination is switched in.)

(If two RS485 ports are needed in a system, or if SERIAL-0 is in use for some other purpose, JED makes RS232 to RS485 converters in 25mm by 50mm by 100mm cases which plug into the SERIAL-0 cable directly.)

Other serial interfaces: I²C

On the same con nec tor used for the two RS232 channels are four more pins allocated for I^2C use.

- SCL, the I^2C system clock; and
- SDA, the I^2C sys tem data.

I^2C operations use a driver supplied by Wilke which sets port addresses on the Ti ger for data- in, data- out and I^2C clock, and the hand book sug gests us ing a di ode in series with the data- out pin to simu late the I^2C open col lector drive. In the TIG501, we route the se lected I^2C clock port pin to the SCL pin, and the data- in and data- out pins are combined onto a bi-directional pin on the Xilinx by pro gram ming an I/O pin as an open- drain out put with simul ta ne ous in put, and this is the SDA pin. (Bits in a Xilinx con trol reg is ter sets up these SCL/SDA pins.)

The I^2C lines have 4K7 pullups.

Because the I2C communications are generated by a CPU un der soft ware, rather than from hard ware reg is ters, the Tiger can be the only "Master" in a system, driving "Slave" pe riph er als. This can in clude other mi cro proc essors with Slave mode support, e.g. some of the Philips 8051 fam ily equipped with hard ware reg is ter I2C sup port can be ini tial ised as "Slave" only I2C de vices.

Note: two Tigers cannot talk to each other via I^2C, as they are both masters.

Other serial interfaces: Dallas 1-wire

In side the Xil inx gate ar ray is logic to gen er ate the appropriate timed pulse generation and sample timing for sig nal sens ing to sup port Dal las "1- Wire" in ter faces. The switched 5-volt output port provide the low-impedance Vcc drive for supporting multiple temperature trans ducers (e.g. the Dal las DS1802) along a "1- wire" net work. (It really is two wires: a ground wire and a sig nal/power sup-

ply line, but Dallas insist this is only "1-wire". We will humour them!) To use the one-wire functions in the Xilinx, it is necessary to link an output port pin and an input port pin on the screw terminal connectors. Multiplexers allow one, two or four terminal pairs to be used for 1-wire runs, allowing each run to be used for different purposes...e.g. one for a multi-sensor temperature monitoring run, one for remote I/O ports and a couple for identification buttons.

The combination of the Dallas interface and the opto-isolated RS485 makes the TIG501 an ideal board for distributing around a factory, building, winery, controlled-atmosphere fruit shed or similar installation, where data can be gathered by a combination of analog and digital means and processed locally or communicated back to a SCADA or PC control site.

Dallas has information about "1-Wire" systems and concepts at: *www.dalsemi.com*
("1-Wire" is a trademark of Dallas Semiconductor.)

Watch-dog timer and RESET generator.

A Xicor X25045 multifunction chip generates a "RESET" to the Tiger and initialises the Xilinx ready for a configuration load on initial powerup, and whenever it detects the Vcc dropping below a 4.5 volt threshold.

This device contains 512 bytes of EEPROM, which can be used to hold any user-defined data. A section of the EEPROM can be hardware write-protected (with a jumper) after programming, containing, for example, calibration data. The device is read and written using serial functions in the Tiger. Non-volatile registers in this device control the watch-dog timer function, and the user program must "tickle" the device before time-out, otherwise a system reset will be generated. The time-out time is user-settable in an internal non-volatile register, but external hardware on the TIG501 disables the watch-dog during PC to FLASH program download, so that time-outs do not interrupt PC-controlled debug operations such as single stepping and breakpointing.

LCD display for text or pseudo-graphics.

Wilke have provided very extensive LCD support in the Tiger, and this is supported by a connector for a 4-line by 20 text display. The software drivers provide user-writable character sets, so pseudo-graphics, bar graphs, etc. can also be displayed.

Keyboard scan and five-key keyboard

The Xilinx gate array provides the logic to match the decoder and scanner system Wilke keyboard scanning software requires...a column of the keyboard is scanned at 1 millisecond intervals, and debounced by the driver. Users can define the ASCII code corresponding to each key co-ordinate, as well as defining control and shift functions or auto-repeat mapping.

A 4 by 5 matrix keyboard scan is provided on connector J6, along with other control panel functions, such as a beeper drive and the status LEDs and LCD display contrast bias control. A 14-pin IDC connector take the keyboard scan across to an external keyboard.

A small PCB, **TIG501KB5**, is available to mount just below the LCD display with five user-legendable 12mm square keys from Greyhill. This small keyboard is intended for use as a menu ing system, with keys used to select between menu items, and a couple of keys allocated for increment/decrement of selected menu items, e.g. setting times, dates or process variables and setpoints.

Analog inputs: 4 channels, 10 bits.

The Tiger has a built-in analog to digital converter, and an external reference, and has a 0 to 4.096 volt range.

A set of four, two-pin socket strips allow users to install their own load resistors (L9) or voltage dividers for wider input ranges (X1, X2), as well as adding filtering of noisy analog sources. A series 10 Kohm resistor is installed, and in conjunction with a 7726 clamper, the input of the Tiger is protected against ESD and 48 volt steady-state signals.

If a 200 ohm load resistor in plugged into the pull-down connector, a 4-20 mA current feeds a 4 volt maximum into an analog input channel.

Assorted other I/O from the Xilinx.

Several other I/O functions originate in the gate array:

- A tone generator with loud speaker driver, able to generate "key-clicks" "beeps" and "alarms" of controllable length and frequency (using a programmable counter in the Xilinx);
- Two LEDs (red and green) which can mount on the TIG501 PCB (halfway along the lower connector strip) or on either the 5-key keyboard or a remotely mounted user-supplied keyboard (the red LED is ON during Xilinx configuration load, and goes OFF when load is successful);
- 5 volt switched "sensor" power to a screw terminal.
- Four switch inputs from a switch along the lower edge of the pcb allow users to enter a 4-bit number for program option selection, or if the RS485 serial multidrop interface is being used, these switches can select one of 16 node addresses.

Battery power for Real-Time-Clock

The 128kB and 512kB Tiger modules include CMOS battey-backed RAM and a seconds-counting Real-Time-Clock. A rechargeable 160 mAH NiMH battery is charged on the board by a resistor-diode combination. This battery is normally mounted by gluing it above the gate array and wiring it to the PCB.

Automatic switching to battery backup is provided inside the Tiger module, but this board does not have system power switching controlled by the clock. The alarm pin from the Tiger (an open-drain output) is available on a pad if users wish to add Tiger alarm-output controlled power switching. (Note: the TIG505 does incorporate such circuitry.)

Power regulator.

Screw terminals at the left of the PCB, and a five volt regulator allow the TIG501 to run from an external 6 to 12 volt power source. Power consumption is 100 mA.