



# JED MICROPROCESSORS PTY LTD

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## (Preliminary)

The BASIC Tiger and Tiny Tiger microprocessor modules present an easy way for builders of embedded control systems to build, program and put small systems into production. The modules are available in a range of memory capacities: BASIC Tigers are available with up to 4 MB of FLASH and 2 MB of RAM inside. Tiny Tigers can have 128kB/32kB, 128kB/128kB or 512kB/512kB respectively. (This board uses the smaller Tiny Tiger).

With this board, JED takes the Tiny Tiger module and places it on a 11cm by 15cm board to make it easy for scientists and engineers to use the Tiny Tiger without having to design a printed circuit board. The board has a Xilinx XC5204 gate array and input protection or FET drivers between the Tiger and all the I/O screw terminals, isolating the Tiger from the outside world for ESD and EMC purposes. Tiger pins are bypassed to a grounded PCB plane, and all supply rails are EMC filtered.

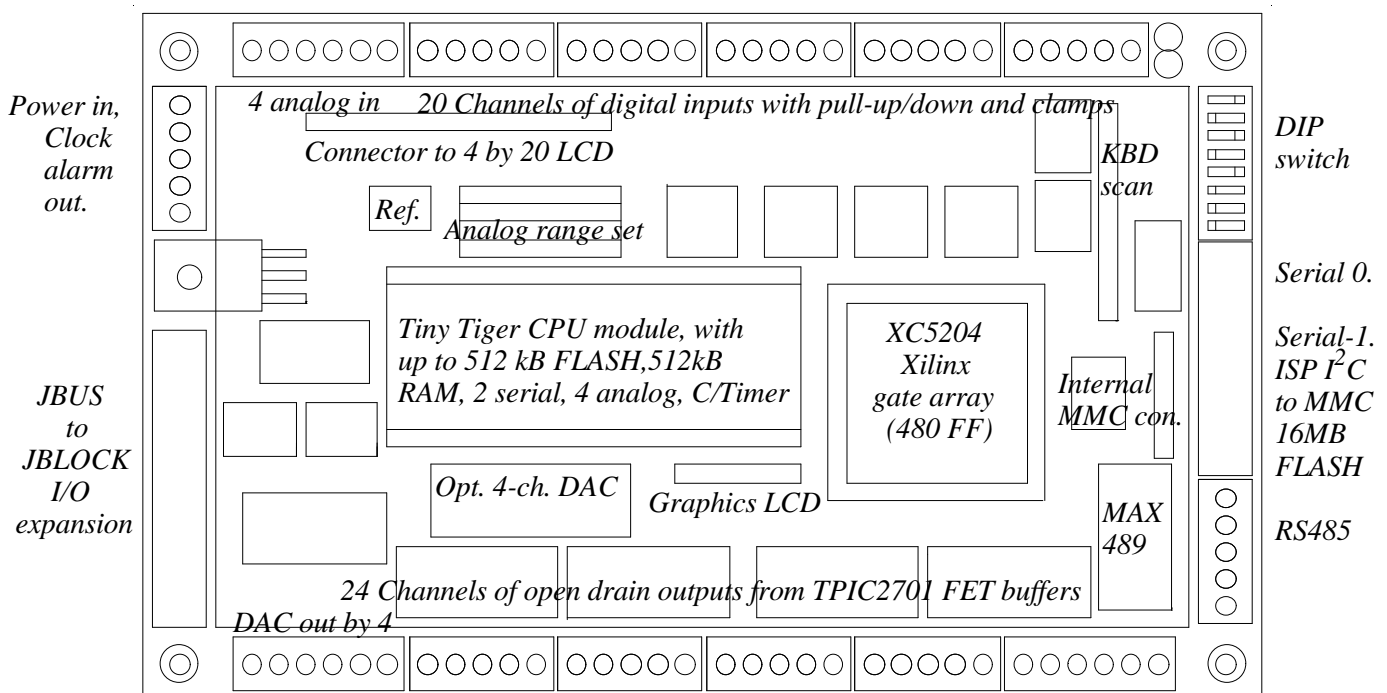
The Xilinx can be reprogrammed by users downloading a data file from the FLASH, so users can re-wire the system between the pins and the Tiger, adding their own counters, pulse generators, shift-register filters, etc.

Users of this board have 20 logic input terminals, 24 outputs with open-drain FETs and four, 10-bit analog inputs. There are two serial ports for communication.

This board can be used as a conventional "single-board-computer", can have a 4-line by 20 character LCD added on top, or can mount behind a panel as a smart controller.

## TIG505, Tiny Tiger controller board for scientific and industrial applications.

- Uses Tiny Tiger from Wilke Technology (Germany), and allows high-performance systems to be developed at low cost, direct from a PC;
- Low power: Tiger draws only 45 mA;
- BASIC multitasking allows modular development of programs with controlled interaction between segments. (Up to 32 tasks allowed);
- Powerful development system runs under Windows, edits, downloads to FLASH and remotely debugs target at source level;
- JED board made in Australia to support the Tiger is first of a family to allow "screwdriver" building of systems, with gate-array reprogrammability of hardware in a Xilinx gate array.



## The Tiger concept and EMC.

The BASIC and Tiny Tigers are small, high-speed microprocessor modules with the high speed bus and memory system housed in a plastic housing, ready to use in applications without users having to worry about the intricacies of high speed bus timing, decoding or paging and addressing. The interfaces necessary for a standard small microprocessor system, (dual UARTs, a complex counter-timer system, plenty of memory (FLASH and CMOS, battery-backed RAM), Real-Time-Clock and an analog input system) are all housed in the module.

Because all the high-speed busses occupy a small volume, RF radiation is very much reduced over a system where the busses occupy a large PCB surface area acting as an antenna. All I/O lines from the Tiger are bypassed to the large ground plane on the back of this board, so any RF which escapes via device pins is bypassed before it can radiate. Supply lines are also L-C filtered.

Please refer to the Tiger data for more information.

## Memory system and download mode.

The TIG505 board can have a choice of three different Tiny Tigers installed:

- TNN-R/1, with 32 kB static RAM, 128 kB FLASH. (This unit has no Real-Time-Clock);
- TCN-1/1, with 128 kB static RAM, 128 kB FLASH, and includes a Real-Time-Clock; and
- TCN-4/4 with 512 kB of RAM and FLASH and RTC.

The choice obviously depends on program size, but users should be aware that if an LCD display is used, the complex device drivers only allow about 10 kB of RAM for user data, and so most users, except for very price-sensitive projects, will be well advised to use the TCN-1/1.

Download to the FLASH occurs when the compiler program (running on the PC connected to a serial port) detects a download request. The Tiger must have the PC switch set to PC mode as RESET is triggered.

## Xilinx gate array and options it provides.

A Xilinx XC5204 gate array in a 160 pin package provides the TIG505 system with 124 I/O lines and 120 Configurable Logic Blocks, (with four flip-flops and function generators each). It is a low-power, RAM-based gate array, so after power-up or reset it is necessary for the Tiger to run a small program to load the configuration bit map into the Xilinx. The file is loaded into the FLASH by a DATA statement in the program at compile time, and the Xilinx loader program reads it from there and loads the Xilinx. (This takes about a second).

There is sufficient space in this device for quite a lot of logic: it can be designed on a screen using schematic entry software and routed using the Foundation low-cost development package from Xilinx. The advantage of such a configurable hardware system is the one PCB and I/O system can have its hardware completely redesigned or altered in quite simple ways. Also, once the board or control system has been tested for EMC with a worst-case design, alterations in the gate array need no recertification.

## Input system, on 20 screw terminals.

Across the top of the TIG505 board are twenty general-purpose input connectors. Input lines can be pulled up to Vcc or down to ground with a resistor array, usually 4k7. A series resistor connects the input pin to the gate array, with a 7726 active clamp on the line to Vcc and Ground, so that the gate array is not damaged by excess voltages or electrostatic pulses to the pin. Input voltage ranges can range + to - 24 volts continuously but can withstand much larger ESD transients. The threshold is at TTL levels .

This input arrangement allows users to select between a voltage input mode (pull-down resistor to ground), or contact or opto-isolator mode (pullup resistor to Vcc).

The standard JED gate array provides these inputs to readable ports implemented in the gate array.

Considerable power is provided in the Xilinx gate array. Several hundred flip-flops are available to build logic between the input pins and the registers read by the Tiger IN instruction.

For example, incremental shaft encoder inputs can be processed with a pair of cross-coupled flip-flops decoding the two 90 degree phase shifted optical sensors into a "count" and a "direction" signal, and then a 32-bit up/down counter can record absolute position into a 32-bit latch and tristate buffers onto the data bus. Control logic can be implemented to control the transfer from the counter into the capture latch, ensuring it is done clear of any input transitions. There is room for a number of such 32-bit encoder processors in the standard XC5204 Xilinx, but larger (i.e. more logic block) devices can be loaded on special request. An XC5210 device has 1,296 flipflops and function generators.

The PLSOUT instruction in the Tiger (Port P86) is routed on the board to a global clock on the Xilinx, and so can be used to generate time bases for counters and timers implemented in the gate array. This is programmable over a wide range of frequencies, up to 2.5 MHz.

## Output ports, on 24 screw terminals.

The outputs consist of power FETs with the sources grounded and the drains connected to the terminals. Each output has a flywheel catch-diode to a zener to 39 volts. The driver is a TPIC2701, with a pull-down resistor on the gate of each FET to ensure it is OFF with the gate array uninitialised on RESET.

The standard gate array allows the FETs to be driven 8-bits in parallel as three 8-bit ports, using the OUT instructions, which include masks allowing individual bits or groups of bits to be addressed without affecting others in the same port. Users can add their own driving logic in the Xilinx gate array. This can include counter and pulse generation logic, to, for example, drive stepper motors.

Four of the digital output screw terminals can be taken over for a 4-channel analog output function (see later.)

## Serial ports, RS232 and RS485.

A 20-pin connector at the right-hand end of the TIG505 has its first 9 pins allocated for SERIAL-0 RS232 port,

wired as a DTE (i.e. the same as a PC would pinout to a D9 connector) A null-modem cable is necessary to connect this port to a PC, but it can connect to a modem (D9 or D25 via an adaptor) directly. The Tiger supports CTS/RTS handshake with the SERIAL-0 driver, but the other RS232 lines terminate in ports in the Xilinx and are readable or settable by IN or OUT instructions. (Ring detect RI has a discrete receiver connected to the power control logic so a sleeping system can be awakened by a phone call and the call answered.)

SERIAL-1 RS232 has three wires on the connector, and this connects to the PC for download. Download mode from the PC is selected by the PC/RUN switch, and inside the gate array this switch overrides the SERIAL-1 to RS485 selection during download and single-stepping.

Switches in the DIP switch select RS485 for either port, and this can be a simple driver chip, or can be opto-isolated. As standard, a MAX489 driver is installed, providing full duplex 4-wire communication to the 5-pin screw terminals. If opto-isolation is required, a **T505IS485** module is installed into the MAX489 socket. The same 5-pin screw terminals are used to the RS485 lines. (No terminations, biasing or 4-wire to 2-wire shorting is provided, as it is assumed users will do this externally if required.)

The Tiger has built-in TX-On control in the RS485-mode driver package for either serial port. RTS0 is used for SERIAL-0 and a port-8 pin connected to the gate array is used as TX-On for SERIAL-1 if it is selected for RS485.

(If two RS485 ports are needed in a system, or if SERIAL-1 is in use for some other purpose, JED makes RS232 to RS485 converters in 25mm by 50mm by 100mm cases which plug into the SERIAL-0 cable directly.)

## Other serial interfaces: SDI-12 standard

The RS485 connectors mentioned above provide a way of incorporating a variety of other serial standards.

The SDI-12 standard is a multidrop sensor standard used by the hydrography and meteorography industries, for communications to up to 10 sensors on the three-wire cable with data tristated onto a five-volt bus with controlled impedance, and a 12-volt cable supplying sensors. If interest exists, we plan to produce a plug-in called **T505SDI-12** to plug into the RS485 socket and users can connect to the SDI-12 cable via the 5-pin screw terminals. (Data on the SDI-12 interface is available on the internet at: [www.sdi-12.org](http://www.sdi-12.org))

## Other serial interfaces: Dallas "1-wire"

Another plugin planned uses the Dallas Semiconductor DS2480 serial to 1-Wire line driver.

This Dallas system converts serial data from a serial port in the Tiger to the 1-Wire system, allowing it to communicate to multiple temperature sensors (e.g. to the DS1820 devices) along one cable, placed around tanks in a winery, for example. Other devices are identification buttons for security systems, etc. The part number will be **T505DS1W**. Dallas has data at: [www.dalsemi.com](http://www.dalsemi.com) ("1-Wire" is a trade mark of Dallas Semiconductor.)

## Other serial interfaces: Microwire/SPI/I<sup>2</sup>C

The Tiger supports clocked data transfers directly from BASIC to user-definable port pins. The TIG505 gate array routes suitable port pins to a user connector: the upper 8 pins on the 20-pin serial connector. These pins are driven by the Xilinx, with 8 mA drive available, via a CMD PAC1284 EMC filter and ESD protector, with 4K7 pullups to 5 volts. The 8 lines on this connector are:

- Vcc and Gnd;
- Clock for Microwire/SPI;
- Dout (from the Tiger);
- Din (to the Tiger);
- CS0\*, low true to select a chip to shift data in/out;
- CS1\*/SCL, usable as a second chip select or I<sup>2</sup>C clock;
- CS2\*/SDA, usable as a third chip select or I<sup>2</sup>C data.

The clocked serial transfers from the Tiger allow the user to set data transfer length (up to 32 bits), and the order of the bits (MSB or LSB first). An OUT instruction to the Microwire/SPI/I<sup>2</sup>C serial control register in the Xilinx controls the CS line for the addressed chip .

Two more chip selects come from the Xilinx register:

- CS3\* and the Clock/Data/Vcc/Gnd lines connect to an internal connector for a MMC FLASH drive; and
- CS4\* is used for a communications with a Xicor X25045 EEPROM/Watchdog/RESET generator chip.

I<sup>2</sup>C operations use a driver supplied by Wilke which sets port addresses on the Tiger for data-in, data-out and I<sup>2</sup>C clock, and the handbook suggests using a diode in series with the data-out pin to simulate the I<sup>2</sup>C open collector drive. In the TIG505, we route the selected I<sup>2</sup>C clock port pin to the SCL pin, and the data-in and data-out pins are combined onto a bi-directional pin on the Xilinx by programming an I/O pin as an open-drain output with simultaneous input, and this is the SDA pin. (A bit in the Xilinx serial control register sets up these SCL/SDA pins.)

The CMD PAC1284 provides 4K7 pullups on these lines, as well as EMC and ESD protection. (Because the I<sup>2</sup>C communications are generated by a CPU under software, rather than from hardware registers, the Tiger can be the only "Master" in a system, driving "Slave" peripherals. This can include other microprocessors with Slave mode support, e.g. some of the Philips 8051 family equipped with hardware register I<sup>2</sup>C support can be initialised as "Slave" only I<sup>2</sup>C devices.)

## Plug-in MMC removable FLASH Disk

SanDisk Corporation have recently released a FLASH disk card they call "Multi Media Card" or "MMC". This device is 24mm by 32mm by 1.4mm thick and has a much simpler interface than PC-Card or camera-style FLASH disks...rather it has only seven surface wipe contacts on the face, and a very simple socket is needed to connect to it. The interface is SPI, and it plugs into the internal connector described above, enabled from the CS3\* line.

The **T505MMC** board connects via a flying line to this connector, and, as the MMC is a 3-volt system, this

interface converts all signals to and from 3 volt levels, and regulates a 3 volt power supply for the MMC. One MMC can hold between 2 MByte and 16MByte.

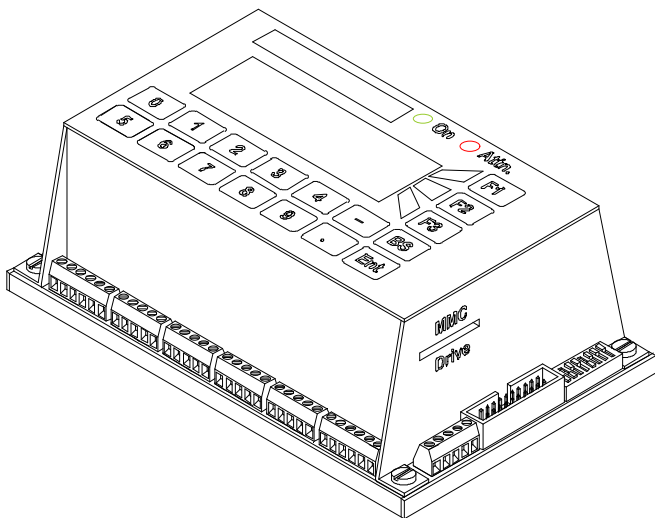
Mechanically, this module can mount in the end of the case of the panel or gear-plate mounting versions.

Additional external drives can be daisy-chained along the cable from the 20-pin serial connector, using chip selects CS0\*, CS1\* and CS2\*, so one TIG505 can potentially have 64 MByte of FLASH on-line and removeable. MMC modules can be written and read with a simple PC printer port adaptor.

### Watch-dog timer and RESET generator.

A Xicor X25045 multifunction chip generates a "RESET" to the Tiger and initialises the Xilinx ready for a configuration load on initial powerup, and whenever it detects the Vcc dropping below a 4.5 volt threshold.

This device contains 512 bytes of EEPROM, which can be used to hold any user-defined data. A section of the EEPROM can be hardware write-protected after programming, containing, for example, calibration data. The device is read and written via the SPI interface, and CS4\* is used to enable communications. Non-volatile registers in this device control the watch-dog timer function, and the user program must "tickle" the device before timeout, otherwise a system reset will be generated. The enable and timeout time is user-settable in an internal non-volatile register, but external hardware on the TIG505 disables the watch-dog during PC to FLASH program download, so that timeouts do not interrupt PC-controlled debug operations such as single stepping and breakpointing.



*LCD/keyboard option for TIG505*

### LCD display options: text or graphics.

Wilke have provided very extensive LCD support in the Tiger, and this is supported by a connector for a 4-line by 20 text display, supported by a 4x5 keyboard scanner. Software and connectors also support a 128 by 240 graphics display, in text and graphics modes.

The box shown in the figure (above) mounts on a gear plate. A similar metalwork version is planned to mount behind a panel with rear-facing connectors.

### JBUS parallel port for expanded I/O.

A 26-pin connector at the left-hand end of the TIG505 provides a buffered JBUS port to the system. JBUS is a JED standard used for communicating on a 26-pin ribbon cable with a range of I/O modules called "JBLOCKS". The bus consists of 8 bits of bidirectional address/data, and address, read and write strobes, generated by the Tiger's IN and OUT instructions. All bus I/O lines are EMC filtered and ESD protected by CMD PAC1284.

### Printer port driver via JBUS port.

The Tiger can drive a parallel printer, and in the TIG505 the JBUS port can be used for this, with strobe lines on the 26-pin connector being routed in the gate array from the Tiger port lines designated in the driver as the printer "data strobe" and "busy" lines. A pin scrambler cable is needed to wire the data bus and strobe lines on the JBUS port to the appropriate printer input lines.

### Analog inputs: 4 channels, 10 bits.

The Tiger has a built-in analog to digital converter, and an external reference, and has a 0 to 4.096 volt range.

A set of four, eight-pin socket strips allow users to install their own load resistors or voltage dividers for wider input ranges, as well as adding filtering of noisy analog sources. In all cases a series resistor of at least 10 Kohm is recommended, and in conjunction with a 7726 clamper, the input of the Tiger is protected against ESD and 48 volt steady-state signals.

### Optional analog outputs, 4 chan., 8 bits.

In place of the left-most 4 digital outputs, four analog outputs can be substituted. Data is written in parallel to a MAX506 8bit DAC and the outputs are amplified to drive the screw terminals. The full-scale output voltage can be set by user-installed gain-setting resistors. (The upper limit is set by the DC input voltage.) Outputs are protected with zener clamps and polyfuses.

### Assorted other I/O from the Xilinx.

Several other I/O functions originate in the gate array:

- A tone generator with loudspeaker driver, able to generate "key-clicks" "beeps" and "alarms" of controllable length and frequency (using a counter in the Xilinx);
- Two LEDs (red and green) which can mount on the PCB (top right corner) or in the membrane keyboard;
- LCD backlight control, ON/OFF;
- LCD bias (contrast) allowing users to adjust LCD viewing angle, and save in the EEPROM; and
- 5 volt and 12 volt "sensor" power to screw terminals.

### Power and On/Off control.

Screw terminals at the left of the PCB, and a five volt regulator and power control logic allow the TIG505 to run from an external 5 volt source, or a 6 or 12 volt source. Power consumption is estimated as 100 mA.

Power switching allows the system to power-down and wake up from a RTC alarm, a keyboard button push or Ring-In from the serial port from a modem.