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STD-801
CMOS Single Board Computer

The JED STD-801 CPU card is designed to provide system developers with a CPU card usable either as a single card computer or as the main computing element in a multi-card system made up of a number of STD bus cards in a rack.

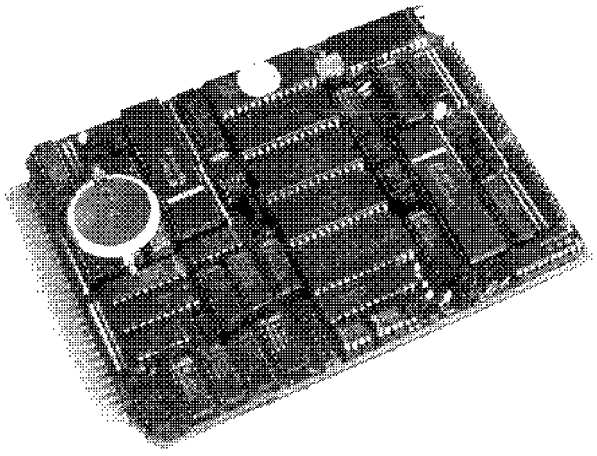
This Australian designed and manufactured computer is intended for a range of applications: Its low power consumption (approximately 90 mA, i.e. 0.45 watt, from a single 5-volt supply) makes it ideal in field data logging applications. It is equally usable in industrial, commercial and educational applications where the reliability of CMOS and the standard Z80 instruction set, combined with both an operating system emulation (for high level compiled languages) and a powerful control BASIC interpreter and monitor make it easy to use.

The card includes parallel I/O, dual serial (RS232) I/O, an optional RS485 interface, 8 analogue inputs (8 or 10 bits), a Real Time Clock, EEPROM, RAM, PROM, three 16-bit counters, a watchdog timer and full STD bus interfacing.

Program development is easy with this card: simply connect a terminal (or the JED STD-850 video board) and type in a BASIC program. When the program is functioning correctly, plug the JED PROM programmer into the top end of the board, transfer the program into PROM, and plug the PROM(s) into the USER sockets. Alternatively, a memory image of the program can be transferred back to the PC and placed into PROM using the JED PC-based programmer.

Machine code debugging is easy using JMON, with breakpoints and the single step monitor command. Cross-compiled programs in a variety of languages are easily downloaded from a development PC or CPM system.

- All CMOS system using National NSC-800 CPU for full Z80 compatibility.
- XTBASIC or C cross-compiler debugger built into system PROM, along with BDOS-BIOS, all I/O drivers and JMON.
- Dual UART serial I/O, RS-232 and RS-485
- Clock/calendar with timer power-up.
- Up to 120 Kbyte of CMOS RAM or PROM, battery-backed with low-profile lithium cell.
- On-card digital I/O (30 lines), 10-bit ADC (8 channels), LCD/LED/Keyboard I/O.
- STD bus expansion for large systems with cards from JED or many other world-wide manufacturers.
- Three 16-bit counter-timers plus watchdog.



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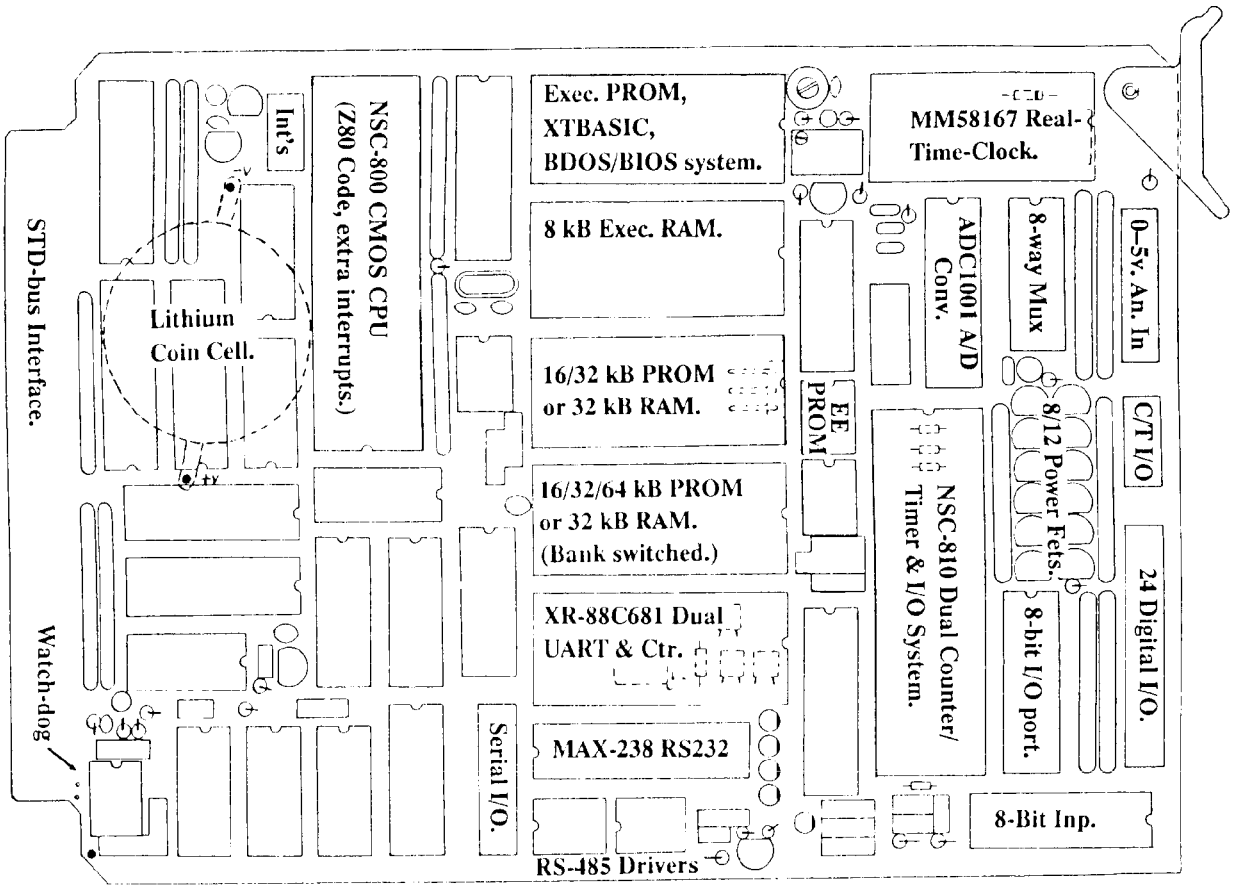

Layout of the JED STD-801 CMOS Single Board Computer

The card uses the National Semiconductor CMOS NSC800 CPU, running at a 4.0 MHz clock rate, along with a number of other CMOS LSI peripheral chips, memory devices and STD bus interfacing.

This CMOS CPU emulates the ZILOG Z80 CPU instruction set completely and exactly. Thus all Z80 software, operating systems, compilers, etc all work in exactly the same way, and instruction timing (for an equivalent internal clock frequency) is identical, including the automatic insertion of a wait state into INPUT and OUTPUT instructions.) The crystal oscillator (on chip) actually runs at twice the CPU clock frequency, but the divided internal clock frequency is output from a CLK pin.

The bus at the chip pins is different from the Z80: it follows the Intel 8085 by multiplexing 8 bits of address information onto the data bus, and generating an address strobe. This is done to free 7 pins which are used to add three more on-chip vectored interrupts (used on the STD-801 for on-card interrupt sources like the timers, UART and real time clock), two status lines, the clock output and a power-save input. The Z80, 8085 and the NSC800 are compared in more detail in National Micro-briefs 3 and 4, available from JED.

On this card, the address is latched, and at the STD card connector the STD CMOS specification is met. The card uses HC CMOS devices throughout, and on the bus pins, the HC driver devices are rated at 6 mA, source and sink. All bus lines are pulled up with 4k7 resistors, so the card is compatible with both LS-TTL and CMOS STD peripheral cards.

It supports MEMEX and IOEXP expansion of memory and I/O space, and all on-card memory can be selectively disabled to allow the card to use off-card memory in appropriate areas on a bank-switched card like the JED STD-816. This memory card can be paged into the memory area 8000-BFFF hex, and several Mbyte can be accessed there.

On Card Memory. On the CPU board are four 28-pin memory device sockets. It is possible to fit up to 120 Kbyte of RAM/PROM into these, using selective bank switching.

In the top 8 kB (address E000-FFFF) is the Executive EPROM, a 27C128, 16 kB device, providing JMON, a powerful monitor, and the BDOS-BIOS system. Transparent bank switching accesses built-in PROM programming software and an INTEGER BASIC interpreter, XTBASIC. An alternative PROM contains the C language debugger.

The next socket is always supplied with an 8 kB CMOS battery backed RAM, which occupies the address range of C000 to DFFF.

There are two more ''user'' 28-pin sockets which each can hold CMOS or NMOS PROMs or RAMs. There are three link-selected maps for this memory:-

- USER1 is 16Kbyte of PROM from 0000-3FFF (a 27C128)
  USER2 is another 16 Kbyte PROM or a bank-switched 32 Kbyte RAM in two 16 Kbyte pages.
  The range 8000-BFFF is off-card, allowing for a RAM/PROM card like the STD- 816, which can hold up to 1 MByte of battery-backed bank-switched RAM.

- USER1 is a 32 kB RAM (during development), then a 27C256 PROM in the final system (from 0000-7FFF). USER2 is either a bank-switched 32 kB RAM, in two, 16 kB pages, (ideal for holding logged data), a 27C256 PROM in two pages or a 27C512 PROM in four, 16 kB pages. USER2 occupies address range 8000-BFFF.

- USER1 is a 27C512 PROM of which 48 Kbyte is used as linear address space in addresses 0000-BFFF hex.
  USER2 is a 32 Kbyte RAM which is only accessible via a special ''hyper-RAM'' mode, in which protected data is written and read via special subroutines.

On Card EEPROM. A 1 Kbit NMC93C46 EEPROM is included on this board, with appropriate control logic. This 5-volt only electrically erasable device holds start-up configuration details like baud rate, I/O devices or locations in a network. It can be read and altered by the JMON monitor or from user programs, which allows users to hold variables like calibration coefficients or offsets.

On Card Dual Serial I/O. Two UART-driven serial communication channels are provided on the board, implemented by a CMOS dual UART chip, the XR-88C681.

This device has its own baud rate generators, and both transmitters and receivers, as well as a 16-bit counter-timer, can generate interrupts, which can be masked and controlled internally and used to generate communications related interrupts to a vectored CPU interrupt input.

The PROM contains interrupt-driven serial communications routines for both UARTs, with user-selectable protocols and buffer sizes.

Usual baud rates to 19200 are supported, with selection between four (usually 300, 1200, 4800 and 9600) being done with plug-in jumpers, and the allocation of baud rates corresponding to jumper positions is done from the non-volatile EEPROM at startup.

Level translation to +/-10 volt RS232 levels for the two transmit lines, and the two RTS lines is provided by a MAX238 device which generates the RS232 levels with two built-in inverters, one from the 5 volt rail to +10 volts, and one from +10 to -10 volts. This device also includes four receivers which handle the two serial data inputs and the two CTS inputs.

Optional RS485 TX/RX I/O. Channel B can be alternatively connected as an RS485 I/O port. Two transceiver chips are provided, allowing for four-wire (full duplex differential pairs in each direction) or two-wire party-line, with RTS control of the connect-to-line function.

(JED manufactures separate boxes for opto-isolated communications, intended for industrial communications interfaces.

The STD-990 is a 20-mA current loop interface, providing TX and RX channels, which can be used independently or connected in series for a single loop.

The STD-995 family are opto-isolated RS232 to RS485 bi-directional interfaces, which allow a serial channel on an STD-801 to be coupled to four-wire or party-line systems.)

On Card Real Time Clock. A battery-backed MM58167AN real time clock chip, with its own 32 Khz crystal oscillator is included. This provides timer registers from hundredths of seconds to months of the year accessible by the CPU, so that time can always be read and known by a program. As well, this chip provides a block of RAM and a multi-way comparator to generate an interrupt on a future time occurrence. Interrupts can also be generated at fixed rates from tenths of seconds to once a month.

The MM58167AN also outputs a control signal which can be used to power up a resting system at the scheduled time, a feature needed for remote site data logging equipment. A separate FET output is paralleled with this line, and allows users to control system powerup and powerdown.

On Card Analogue Input. For analogue input, either an 8-bit or a 10-bit analogue to digital converter is provided. The ADC0803 or the ADC1001 converters allow the CPU card to do data gathering or monitoring without needing additional cards. In front of the converter is an 8-channel analogue multiplexer with latch. This allows 8 analogue input lines to be scanned. If more channels are needed, the parallel I/O lines (see below) can control a pre-card multiplexer. The normal input range is 0-5 volts, but JED makes a variety of front-end boards for thermocouple and other low-level signal inputs which can be added in front of the STD-801.

The conversion time is 100 microseconds for the 8-bit converter and 200 microseconds for the 10-bit device.

The conversion is stable even in the noisy CPU environment because a WAIT state is generated to the NSC-800 during the actual conversion time.

NSC810 Parallel I/O, and Timers. This LSI chip adds two programmable 16-bit counter timers to the system. They work in six modes, have a pre-scaler, and can generate interrupts if required. They can be linked to external inputs or the CLK signal, so they can be used to monitor and count signals such as tachometer pulses, outputs of metering devices for gas, water or electric flow transducers, or to generate pulses, tones or time delays before interrupt.

The device also provides two 8-bit and a 6-bit I/O port with direction control registers and easy bit-control. These lines, and an additional 8-bit input buffer provides 30 bits of I/O to the basic card. These are at the top end of the card with a 26-pin and a 10-pin ribbon cable connector, allowing the card direct control of the outside world.

Normally eight of the output lines are buffered with VMOS power FETS, with a 60 volt, 200 mA rating, allowing relays to be driven. Four more FETs can be installed on four of the 6-bit I/O port lines if other functions on these lines (like counter gating) are not needed. Another 8 bits are used as a bi- directional port with HC CMOS or a 74LS245 as the I/O device. A (separate) third port consists of 8 inputs. These two 8-bit ports have 4k7 pull-up resistors to allow switch or logic inputs.

Summing up, parallel I/O on this card consists of 8 bits of input, with 4k7 pullups, 8 bits of bi-directional I/O at TTL/CMOS levels (with 4k7 pullups), 8 bits of power driver output and 6 bits of low-power I/O combined with other functions, 4 lines of which can also be FET buffered.

PROM Programming. The 26-way connector used for parallel I/O provides connection to the JED PROM programmer box (Rev C), and allows programming 2764 up to 27512 NMOS and CMOS PROMs.

(Alternatively, a .HEX image file can be generated by the JMON monitor and saved back on the PC, from where a PROM can be generated using the JED PC-based PROM programmer.)

Parallel Printer. The parallel I/O ports can also drive a parallel printer, and the PROM contains driver and select routines for this.

Microwire I/O to DataSafe and Displays. A separate 10 pin connector on the board connects the output of a latch and an

input line to external serial I/O devices with Microwire compatibility. Microwire is a National defined serial protocol which provides enable, clock and data IN and OUT lines to enable the system to communicate via very few wires with a range of multi- digit displays (LED, LCD, etc).

Four display devices interfaced via this microwire port are supported as I/O devices by JMON BDOS-BIOS and XTBASIC. These are:

- The NSM4005A, a 4-digit 0.5" LED display module,
- The JED STD-965, a 4-digit 7-segment LCD display,
- The JED-860, a two-line or four-line by 40 character LCD dot matrix display and keyboard interface, and
- The JED-960 a 8 line by 40 character or 64 by 240 dot graphics display, with a QWERTY membrane keyboard.

This port is the method the card uses to send serial data into, and to get it back from, the JED DataSafe device, for off-card bulk storage in CMOS RAM of either programs or field data.

JMON Monitor. A resident monitor program, JMON, has been written specially for this card. It is supplied in the EXEC 16 kB EPROM, which also contains the BDOS-BIOS emulation and the XTBASIC interpreter.

JMON provides data display, moving, loading and dumping (in CPM/Intel .HEX format) and program debug facilities (including NMI controlled SINGLE STEP of machine code programs.) It provides standard I/O entry points for multiple interface devices, and controls device initialization by reading the EEPROM on start-up and calling selected device initialization routines. User provided device routines can be easily integrated into this system via vectors added into the EEPROM.

XTBASIC Interpreter. The executive PROM contains a specially adapted INTEGER BASIC. This has functions for time and alarm setting and reading, direct analogue input and BIT and BYTE manipulation.

Its execution speed is relatively fast: about 1000 lines per second. (It is actually faster than Microsoft's Z80 BASIC in its fast integer mode.)

Decimal point and formatted PRINT statements are included in XTBASIC, although the maths routines are 16-bit integer.

Simple STRING functions are provided, allowing strings of text to be captured in RAM from external devices or computers and then analysed. Strings in RAM can be formed from any statement valid within a PRINT statement, and these can then be transmitted.

Dynamic re-direction of data I/O device allocation is provided, allowing PRINT and INPUT statements to switch between the current CONSOLE, the AUX-IN and AUX-OUT devices and the PRINT device. PRINT statements can also direct numeric data to the NSM4005A LED displays, and the JED-860 and JED-960 LCD displays are also supported for both input and output.

Thus an XTBASIC program could allow operator entry of commands or data via the LCD display on the front of an instrument, send data in parallel to a local printer or STD-850 video card, or communicate with a remote computer or other instrument via serial interfaces.

The machine language CALL statement allows programmers to call JMON (or user provided) subroutines in a very efficient and unique way, to, for example, send data to the JED DataSafe. All normal Z80 internal registers are imaged directly into XTBASIC variables (e.g. CPUA, CPUF, CPUHL, etc) and so the user can set up any register, CALL, and then examine a register using IF commands, or store results in RAM.

Single dimensional ARRAYs are also supported.

The JED C-language Programming System

The compiler runs on an IBM PC (or clone) under MS-DOS and produces code for the JED STD-801. The compiler includes the standard C preprocessor and ANSI-compatible compiler, a powerful macro-assembler, and a linkage editor. Options supplied on the compiler command line control the operation of the various stages of compilation. The output of the compiler is an Intel hex file that can be transferred to the STD-801 under the control of a communications program.

Standard ANSI C libraries are supplied with the Hi-Tech compiler. Full floating point libraries are included. The JED C System provides additional libraries specifically designed for systems running on the JED STD-801hardware. Code requirements have been specifically reduced, and many functions have been optimized to take advantage of the facilities available on the STD-801.

Using the JED C libraries, the programmer has all the functions required for efficient access to all the features of the JED STD-801. There is no need to write code in assembly language, or to learn the details of operation of the board hardware. Such details are concealed in the library.

Functions are provided for-	Hyperram Access
Full I/O redirection	Real-time clock access
EEPROM access	8,10 and 12-bit ADC access
Watchdog Reset	DataSafe Type 'A'Access

The compiler provides facilities for handling interrupts directly in C. This eliminates the need to write assembly interrupt handlers. The compiler automatically generates the required data entry and exit code, and inserts vectors.

Source codes for all library functions are included on the distribution disks should detailed analysis of the operation of a function be required.

Included in the C system is a cross-debugger that allows C source-level debugging of a program running on the STD-801. The debugger runs on the PC, communicating with a small stub running on the STD-801 in a **C-EXEC PROM**. The debugger allows single stepping in C or assembly, breakpoint setting, disassembly, and stack traces and variable dumps.

The Hi-Tech C compiler is a standard C cross-compiler producing Z-80 code for a CP/M system. The JED C System supplements the Hi-Tech compiler with additional libraries, startup codes, header files, a revised compiler driver program, and a JED- C specific manual.