



# JED MICROPROCESSORS PTY LTD

173 Boronia Rd, Boronia, (PO Box 30), Victoria, 3155, Australia  
Phone: +61 3 9762 3588 Fax: +61 3 9762 5499  
<http://www.jedmicro.com.au> email: [jed@jedmicro.com.au](mailto:jed@jedmicro.com.au)

## AVR573 for plug-in Atmel CPU module

The AVR573 is a base-board to allow users to run the AVR570 ATmega128 CPU module in an application. This module has the surface mounted CPU and a number of other components closely associated with the CPU functions (e.g. the main CPU crystal and reset generator), so users have a means to power and interface the module, and connect it into an industrial, scientific or domestic application.

For users who wish to use the ATmega128 in their own application without the complexities of surface mounting the CPU, the combination of the AVR570 surface mount module, available as a pre-assembled and pre-tested function, with the AVR573, available as a kit for hobby or academic users provides an ideal combination.

The 573 base-board is 100mm by 160 mm with mounting holes in each corner to stand the board off of a base plate. The I/O connections are along the upper and lower edges, and keyboard and LCD connectors are at the right-hand end. The board layout drawing shows the labels of all the connections and their functions.

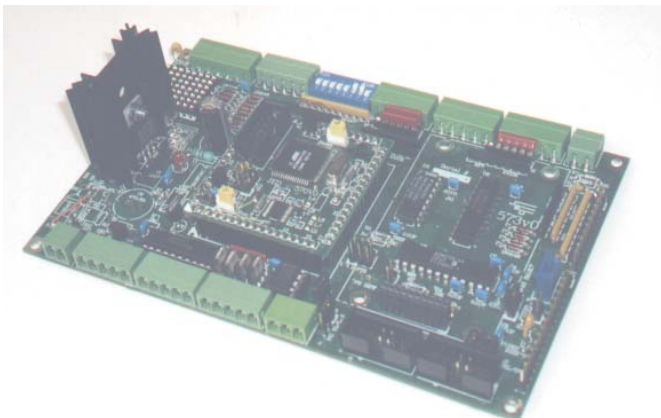
## Functions on the AVR570 module

Reference should be made to the separate data sheet available for the AVR570, which gives layout and details of the AVR570, but in summary, the functions provided are:

- ATmega128 CPU with 128K Bytes of FLASH program memory, 4K Bytes of RAM memory and 4K Bytes of EEPROM non-volatile memory;
- Six-pin programming header for programming the CPU FLASH and EEPROM via the programming dongle from a PC. JED makes the J956 programmer;
- Slide switches for RESET and PROGRAM/RUN functions;
- Reset\*/low-Vcc controller;

## AVR573 CPU card, with ATmega128-based JED AVR570 Module

- High speed RISC CPU with 128K high-security FLASH program memory, 4K Byte of SRAM, 4K Byte of EEPROM, with 133 instruction set, superb C and BASIC support;
- AVR573 is base-board to hold JED AVR570 module. All surface mount components are on module, and AVR573 is all through-hole, allowing easy customisation of small quantities, or TAFE and hobby project use;
- Two UART interfaces, feeding two RS232 or one RS232 and one RS485;
- Twelve inputs, twelve power FET outputs;
- Eight analog inputs, with termination and scaling resistors. Low temperature-coefficient reference for 10-bit CPU ADC ;
- On-board mountings and connections for Global Positioning System;
- Expansion connector for I<sup>2</sup>C or SPI clocked serial bus, either on or off CPU board;
- Choice of two on-board 5 volt regulators, linear, or switching for 6/12/24 power input;
- Optional Real Time Clock (DS1305) , with on-board lithium battery behind board, able to start a sleeping system via alarm.



Designed and manufactured in Australia by an Australian-owned company.



Users can install their own resistors or capacitors here for input signal conditioning.

Inputs from screw terminals J1 and J2 are fed to two socket positions on these strips, and Ground, Vcc and CPU ADC input pins alternate with the input signals.

Users can install pull up resistors to Vcc or pulldown resistors to ground. A pullup resistor to Vcc can supply power to a sensor such as a Thermistor, an AD590 voltage-output temperature sensor or a grounded resistor sensor such as a fuel or other liquid level sensor. A pull-down resistor to ground can terminate a 4-20mA loop system to measure the current. (A 200-Ohm resistor converts a 20mA signal to 4.00 volts.) The reference-input voltage is 4.096 volts so this gives an ADC count of 1000 for 20mA loop current.

After the positions for the pull-up and pulldown resistors are sockets for a series resistor for CPU input protection or voltage divider use. All analog inputs have low-leakage clamp diodes to ground and Vcc to protect inputs from ElectroStatic Discharge (ESD) or fault-caused out-of-range inputs. Typical input values could be 10K ohm.

If it is desired to handle larger input voltages than the 4.092V input undivided full-scale, additional resistor sockets are provided (at the end of the socket strip) for a CPU input-pin to ground resistor acting with the series resistor as a divider. A 4 to 1 resistor ratio divider would give a 20 volt input range with a count of 1000 corresponding to 20 volts, i.e. 20mV per bit.

If no divider resistor is installed, a filter capacitor can be placed in these last sockets.

(For best accuracy, 0.1% low temp-co resistors should be used for dividers and 200 ohm loads. These are available from JED, RS or Farnell or other resistor suppliers.)

The reference voltage to the CPU ADC on the AVR570 is supplied from a Maxim MAX874CPA, which can be accurately set with a trimpot on the board to 4.096 volts. This gives a reading of 1000 counts for 4.000 volts, i.e. 4 mV per bit.

A 5 volt regulated power outlet is available on the analog input socket J1 pin 1 via a 100mA Polyfuse to supply sensors or pre-processing logic.

## JTAG interface

The AVR570 has pads for the optional connector to the Atmel JTAG debug interface. This is enabled with a fuse bit in the CPU set with the programmer, and when in use, allocates the upper four lines of the ADC port (Port F). Thus if the JTAG debugger is in use, these lines are unavailable for ADC or Port F use. The series resistors in these four lines should be unplugged in this case.

## Digital use of Port F, (ADC port)

The analog input connections discussed here can also be used as 8 additional digital I/O lines. The analog port pins are also wired in parallel with a digital I/O port, Port F bits 0 ... 7, inside the CPU.

As a digital input, pullup resistors can be programmed ON inside the CPU. These are of quite high value, and it is

recommended that external pull-up or pulldown resistors be installed in the socket strips just discussed. Series protection resistors are then installed in the "series" positions in the socket strips to bring the input signals to the CPU port on the AVR570. Clamp diodes protect the CPU. As a guideline, 4.7K pullup and series resistors are a good choice.

As a digital output port, the outputs from the CPU are a totem-pole output with 20mA source and sink drive. If used in output mode, a low value series protection resistor or a zero Ohm link should be installed in the "series" socket positions.

## Digital input system

The digital input system on the AVR573 has twelve input lines to the CPU ports (four to dedicated special function pins), an eight-way DIP switch input and a 6 by 4 keyboard scan system.

Port A of the CPU is shared between eight inputs, the DIPswitch, and the keyboard functions; tristate buffers are enabled and disabled as these latter functions are read. All is controlled by an OUT instruction to the three lower Port G pins.

Setting a "0", "1", "2" or "3" to these Port G bits scans the four rows of the keyboard, and inputs from the six columns of the keyboard are enabled to the Port A bus into the CPU and can be read with an IN instruction. (The top two bits on this keyboard buffer are the DCD and CTS lines of the serial port SER0.)

Setting "4" to these three Port G control bits enables a read of the eight-way DIPswitch via CPU Port A. An ON of a switch is read as a "0" on that bit. (Pads under the DIPswitch allow the switch to be off-board, for example, a thumbwheel switch on a front panel.)

Setting "5", "6" or "7" to these three Port G bits disables the tristate buffers for the keyboard and DIP switch, and 10K Ohm series protection resistors from the J5 and J9 connectors allow input data to be read by the CPU, eight bits wide, at Port A. These input ports have sockets for user-installed quad (5-pin) pull-up or pulldown resistor packs, typically 4.7K Ohms in value. (Pull-up resistors allow a switch or opto-isolator input to be sensed, a LOW indicating a closed contact or active opto-isolator. Pull-down resistors allow for a voltage input to be sensed, where a voltage greater than 2 volts being sensed as logic HIGH.)

The other four inputs for the AVR573 come from the connector J10, and are wired to CPU input pins directly via series protection resistors. The CPU pins have these functions:

- Input 9 is Interrupt Input INT6, and CPU Port PE6. This is also Timer 3 input;
- Input 10 is Interrupt Input INT7, and CPU Port PE7. This is also Input Capture Trigger for Timer 3;
- Input 11 is Timer 1 input, and CPU Port PD6; and
- Input 12 is Timer 2 input, and CPU Port PD7;

These 4 inputs also have sockets for a pull-up or pull-down resistor pack as above.

## Digital output system

There are also two groups in the digital output system:

- Eight low-power FET outputs are fed from a TPIC6259 device, which provides eight, 250mA continuously rated N-FETs with 1.3 Ohm typical channel resistance. These have output clamps at 45 Volts. This device is an addressable latch which has all outputs cleared OFF on RESET, and can have bits set/cleared by placing an address on Port G bits 0, 1 and 2, data 0 or 1 on Port D bit 4, and then taking Port D bit 5 LOW then HIGH to latch an output; and
- Four high-power FETs, MTD3055, driven directly by four CPU pins, Port E bits 2, 3, 4 and 5. CPU Port E Bits 3, 4 and 5 are respectively PWM Counter/Timer 3 Outputs A, B and C. These FETs are rated at 2A continuous on the board, and have internal output clamps at 60 Volts.

## Serial Interfaces

Two UART driven serial ports are provided in the ATmega128 architecture, and these both are buffered on the AVR573 base-board, with two RS232 and a RS485 interface, as well as a TTL/CMOS level interface to the on-board GPS.

As well, SPI and I<sup>2</sup>C (TWI) clocked serial interfaces are provided in the CPU.

### Serial I/O: RS232#0

UART0 in the CPU becomes the RS232#0 interface, and J15 is the connector for this channel. This is pinned out as a DTE (Data Terminal Equipment), so it will connect with a straight-through cable (such as a ribbon cable) to a modem, GSM phone, etc. If it needs to connect to a PC (also a DTE) a "null modem" cable is needed to swap signal and handshake lines.

As well as the TXD0 and RXD0 lines to the port, outputs RTS0 (derived from CPU Port B bit 6) and DTR0, (derived from Port B bit 7) are available. Inputs for the DCD0 and CTS0 lines are also provided, and are read via the keyboard buffer to Port A bits 6 and 7 respectively (when the keyboard is addressed via port G).

### Serial I/O: RS232#1

UART1 in the CPU becomes the RS232#1 interface, and J16 is the connector for this channel. Active lines on this interface are TXD1 and RXD1. These lines go via crossover links on the base-board so the port can be easily configured as either a DTE or a DCE device. No active handshake lines are provided, but another link jumpers RTS and CTS lines. DSR, DTR and CDC lines on J16 are also passively linked.

### Serial I/O: RS485

UART1 serial comms can also be jumpered to transmit and receive via a RS485 interface, as an alternate to RS232#1. This connects to screw terminals J17, with a ground and the differential signal lines. To use the RS485

interface, a jumper on the board must select the RS485 receiver to the CPU.

The CPU must turn on the RS485 transmitter before any characters are transmitted. Because RS485 is a "shared medium" system, the transmitter must be turned off to release the lines for other devices on the RS485 network or to receive a reply from a remote node with which this node is communicating. The TX\_Enable line for the RS485 transmitter is Port B bit 5. The ATmega128 UARTs have a convenient "Transmit Complete" Interrupt, allowing a routine to turn off the transmitter just after the last character being transmitted clears the UART shift register.

## Serial I/O: GPS

If the optional on-board GPS header and support is installed, four mounting studs hold the module, and a 20 pin fine-pitch header interfaces to the pins on the rear of the module. Communication with it is at TTL/CMOS level asynchronous serial at 9600 baud, and uses the CPU UART 0. (A jumper connects the receiver from the GPS to the CPU RXD0.)

Five volt Vcc powers the GPS and Polyfuse-limited antenna power is supplied on another pin. System RESET\* also resets the GPS module.

A second jumper can be installed to connect the unused RS232 RS232#0 receive buffer into the second serial input of the GPS to allow differential GPS correction signals (via J15) to be decoded by the GPS for high-accuracy applications.

## Serial I/O: Expansion on/off board

Connector J14 on the base-board is provided for expansion of I/O for the AVR573, making use of the SPI and/or I<sup>2</sup>C (TWI) interfaces supported by hardware on the CPU. This connector allows for a JED-made prototype board to be plugged in, using the same mounting studs as the GPS would use. This prototype or custom board is a little longer to interface with connector J14. (It can also pick up the GPS connector and use pins on that connector with UART0 TX and RX lines. Thus, for example, a second RS485 interface could be added to this board.)

The main expansion medium on this expansion connector is via the I<sup>2</sup>C and SPI interfaces. Port D Bit 0 is SCL/INT0, and Port D Bit 1 is SDA/INT1.

Several other port pins come to this connector, and these can be used for device or chip select lines for the SPI interface.

### Lines provided for SPI are:

- Port B Bit 0 (SS). This can be used either as a SPI chip select, or for SPI master/slave handshake;
- Port B Bit 1 (SCK);
- Port B Bit 2 (MOSI);
- Port B Bit 3 (MISO).

### Port B, Bits 4 to 7 lines all have other functions:

- Bit 4 can be used as a SPI chip select, or alternatively as the LCD backlight control, as selected by a jumper L18. This jumper can also turn the backlight ON or

OFF permanently (e.g. when this bit is used by an interface);

- Bit 5 can be used as a SPI chip select, but is hardwired to the TX enable of the RS485 transceiver, so should not be used for any other purpose if the RS485 interface is being used on the AVR573;
- Bit 6 can be used as a SPI chip select, but its alternate function is to provide the RTS line on serial interface RS232#0. Selection of this function is via link L13, which disconnects the RS232 RTS driver and grounds the input, sending out a permanent +9 on the RTS line. Bit 6 is then released for use by the SPI interface;
- Bit 7 can be used as a SPI chip select, but its alternate function is to provide the DTR line on serial interface RS232#0. Selection of this function is via link L12, which disconnects the RS232 RTS driver and grounds the input, sending out a permanent +9 on the DTR line. Bit 7 is then released for use by the SPI interface.

Note: If no I<sup>2</sup>C interface is used, Port D bit 0 and Port D Bit 1 (The I<sup>2</sup>C SDA and SCL lines) can be used as SPI chip select lines, or just as general purpose I/O lines. They can even be used as interrupt input lines, as they are INT0 and INT1 input lines.

## I<sup>2</sup>C interface

The I<sup>2</sup>C interface uses the SDA and SCL lines from the CPU (Port D, bits 0 and 1) and a full hardware-supported interface inside the ATmega128 CPU, with clock speed control and interrupt support. Multi-master and slave modes are supported. Series protection resistors and pull-ups for the SDA and SCL lines are provided on the base-board, so J14 could be used as a ribbon cable connector to connect to another board, as well as to the “upstairs” board.

A 4-way ribbon cable from this connector can pick up pins 11 to 14, i.e. Ground, Vcc, SDA and SCL in order. Because addressing is done in the structure of the I<sup>2</sup>C messages sent, and I<sup>2</sup>C chips have addresses either preset inside or set by address pins on the chip. Select lines are not needed.

(Many pages in the ATmega128 data-sheet are devoted to this interface, with sample code.)

## SPI interface

This interface uses Port D Bits 1, 2 and 3 (SCK, MOSI and MISO) as signal lines, and chip select lines from available pins as discussed above.

As with the I<sup>2</sup>C interface, the SPI interface can also be extended off-board by a ribbon cable. J12, Pins 1 and 2 are Ground and Vcc. Pins 3 to 10 are Port B bits 0 ... 7 in turn, leaving the top four pins available for the I<sup>2</sup>C, either on or off board.

## LCD and Keyboard Interface

Connector LCD1 is a 16-pin strip header to go to an off-board LCD display. This runs from Port C, Bits 0, 1 and 2 as control lines, and bits 4 to 7 as a 4-line (2-nibble) data bus for the LCD. This will run any Hitachi 44780 controlled 4 line by 16 or 20 LCD or any 2 line by 16, 20, 32 or

40 LCD. A bias supply for the LCD display is supplied from a trim pot to set the viewing angle. Positive or negative polarities are available and are selected by jumper link L11, to accommodate wide-temperature-range LCD displays.

A link from Port C, Bit 3 is available (via link L17) to provide an additional E line to support a larger, two-controller LCD, such as a 4 line by 40 display.

The keyboard interface was discussed above. It uses codes 0, 1, 2 and 3 sent to Port G to select keyboard columns and then the read of the lower 6 bits as a row into Port A.

## Dallas 1-Wire I-Button

Port C, Bit 3 can be used as a 1-Wire port to a Dallas 1-Wire network with one or more devices from the 1-Wire range. Dallas 1-Wire ports are supported by software in both BASCOM and CodeVision, and the port pin used is setup in the program. Communications are initiated by the CPU driving the line LOW for 500 microseconds to RESET the connected device. ONES or ZEROS are sent with shorter or longer pulses. Commands are sent in as ONES or ZEROS and data is read out by sending in a short pulse, floating the port bit, and detecting whether the connected device releases the line or holds the line LOW for a specified period.

The port is ESD protected by clamp diodes.

## Real Time Clock system, with alarm

There is an option of a Dallas SPI interfaced Real Time Clock on the AVR570 module. This has its own 32KHz crystal and lithium backup battery (mounted on the back of the AVR570, between the printed circuit boards). Two lines from the AVR570 to the base-board allow a P-channel power FET in series with the input power to be controlled by the RTC. Thus an alarm time can be set in register in the DS1505 RTC chip, and when the alarm activates, the board power is switched ON.

A data logging cycle or some other function can be performed, and then a new alarm time set and the board powered down again.

## Power supply system

The input power to the board connects into connector J19. Several different board loadings are available depending on the application and power requirements.

In a simple application running from a mains (plug-pack) or a low voltage battery supply (say, 3-cell lead acid gel cell at 6 volts) or a 12 volt vehicle system, a low-dropout linear regulator, e.g. a LM2931 or LM2940) on a heat-sink is installed, and will operate the system down to 5.5 volts input. The voltage limit of the regulator and the dissipation limit of the regulator on its heat sink determine maximum input voltage in this configuration. The maximum input voltage of the regulator (staying in regulation) is +26 volt. Anything over this voltage, and the regulator closes down. It does have a positive transient protection rating of +60 volts, so if it is used in a +12 volt vehicle system, the regulator is able to withstand load dump pulses.

The regulator is also reverse-protected against continuous voltages of -15 volts and negative transients of -50 volts.

Dissipation limits for the linear regulator system are determined by what power is consumed on and off board. The CPU on the AVR570 module and the logic on the AVR573 board consumes about 60 mA, so if just the CPU system is used (no GPS or large LCD backlight current), the heatsink will run the board with no detectable temperature rise on +12 volts. If this is all the power used, a LM340-5 with higher voltage rating (35 volts) can be used as a medium current linear regulator from even +24 volts, probably with the addition of the series diode and the 30 volt Transorb and series Polyfuse for reverse voltage protection and overvoltage protection.

Power up to 100 mA at can be drawn from pin 1 of J1.

Power is consumed by the backlight of the LCD display, and this depends on whether it is run continuously, or only on demand (e.g. when someone is using the keyboard). The current drawn depends on whether a small or large display is used, and what level it is run at. This could

range from 50mA to 400mA, and is set by the backlight series resistor, which can be changed by users.

Power is also consumed by the GPS at 5 volts, and can be up to 250mA with an active antenna.

### **Switching regulator option**

If a higher current is required at 5 volts (e.g. if a GPS or higher LCD backlight current is installed) an option in place of the linear regulator and heat sink is to install a Nemic Lambda 3 watt 9/18 volt to 5 volt, or a 18/36 volt to 5 volt DC/DC converter, for 12 or 24 volt systems. This runs cool at 3 watts (600 mA output), and does require the reverse voltage diode and Transorb for protection, especially in a vehicular environment.

To reduce the noise associated with switching regulators, a ferrite and feed-through EMC filter is installed on the input side of the DC/DC converter filtering both power and ground input lines. Then, on both the input and output, a pair of 470 microfarad low ESR (Effective Series Resistance) capacitor filters output power to the AVR573 and noise reflected back to the input power source.