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JED TIG515 Economy Tiger based single board computer

The TIG515 is a single board computer designed to fit with a 4 by 20 LCD text display and keyboard behind a panel doing control tasks, or can be cabinet mounted with a cable leading to the display and keyboard. Alternatively, the board can be used without any display or keyboard as a low cost control computer with digital and analog I/O.

Development software...Multi-tasking BASIC Compiler

This board makes use of the recent release by Wilke technology of the new Rev 5 BASIC compiler for the Tiger family, in either a full release form or in the low cost "Lite" version on CD. (The Lite version is limited to 3,000 lines of code, but otherwise is a full release, with all Multitasking features, data types and device drivers supplied.) The software package allows programs compiled on a PC to be down-loaded to a TIG515 board via a simple serial cable, and the code then to be single stepped and debugged without the need for other hardware, programming "dongles", or In Circuit Emulators.

E-Tiger

The "E" Tiger is in a smaller 28 pin package than the Tiny Tiger (without RTC and battery backup on the RAM), but the limited I/O is not a problem on this board, as the E-Tiger is used in Expanded I/O Mode, and there are sufficient pins on even the E-Tiger to support the Bus-mode expansion via a Xilinx FPGA, providing up to 35 analog and digital I/O lines, the LCD display, keyboard scan, two RS232 ports with buffering, an RS485 port, a Dallas 1-Wire port, a 8-switch input port and an SPI expansion port to 4M bytes of on-board FLASH memory for data-logging applications. (There is a battery backed Real Time Clock on the board, implemented externally to the Tiger.)

Mechanical details

The board has two expansion sockets allowing addition of extra I/O, eg analog output ports to screw terminals. These expansion adaptors are shared across a number of JED products, eg the TIG520 and the AVR590 boards.

The board is 160mm by 90mm, with stud mounting holes in each corner, as well mounting holes for two sizes of 4 by 20 LCD display modules. The smaller module is 98mm by 61mm, with 5.5 mm high characters, and the larger one is 146mm by 63mm, with 9.5mm high characters. A 4 by 3 "telephone-keypad" style keyboard is supported alongside the smaller display without needing cables, but a larger, 4 by 5 keyboard can be scanned with a cable connection or a flex-film cable tail used.

Serial I/O for the TIG515

There are two serial ports on the E-Tiger, SER0 and SER1. These are supported under interrupt and the multi-tasking system by device driver software, providing buffers from 256 bytes to 8K bytes of storage on each of the two channels, for each transmitter and receiver. Functions provided allow buffer control, clearing and sizing, 9-bit mode setting and address control for RS485 multi-drop) Xon-Xoff handshake control, etc. On this board, there are two 10-pin IDC connectors for the RS232 ports.

SER0 facilities

SER0 is a DTE pinout if a ribbon cable with a 10-pin IDC female socket is crimped on one end, and a D9 is crimped on the other. This pinout would suit a direct connection to a modem, GSM phone or data radio system

Lines provided are:

- TXD0 output data;
- RXD0 input data;
- CTS0 “Clear to Send” input for handshake. Must be HIGH into the board to allow SER0 to transmit. A link on the board allows this to be always allowed by strapping the input on the Tiger pin fed from this receiver to GND (equivalent to an RS232 HIGH on CTS0). This should also be done when using SER0 for RS485;
- RTS0 “Request To Send” out, fed from a control bit in the Xilinx. This can be forced HIGH on the RS232 output by a link;
- DTR0 “Data terminal Ready” output, from a control bit in the Xilinx, used to indicate to a Modem that a terminal device is connected;
- DCD0/DSR0 “Data Carrier Detect” input, or “Data Set Ready” input (via selection link, into Xilinx input).

SER0 can also be used for RS485 (see below).

(It is also possible to use this interface for communication and power of the JED DS603 serial DataSafe, a serial memory device which could be written from this card and read without adaptors or power by any PC via a serial port.)

SER1 facilities

SER1 is a DCE pinout if a ribbon cable with a 10-pin IDC female socket is crimped on one end, and a D9 is crimped on the other. This pinout pins directly into a PC serial port or other serial terminal device. It is used for program downloading of the Tiger from a PC via the Wilke compiler or downloader software. (A switch, labelled “PC” selects this function)

Lines provided are:

- TXD1 output data;
- RXD1 input data;
- Loopback of DTR1 in to DSR1 and DCD1 out;

- Loopback of RTS1 to CTS1.

SER1 can also be used for RS485 (see below).

RS485/TTL serial facilities

A 5-pin screw or plug in Phoenix connector provides four-wire or (with links) two-wire RS485 communications. This is a long-distance (up to 4,000ft) multidrop communications system using differential signalling, and this board can handle a variety of protocols, including standards such as Modbus. The Tiger device driver allows setting of a Tiger pin as a controller for the TX enable of an RS485 network, so it turns the RS485 transmitter ON just before a byte is transmitted and turns it OFF just after the last byte is cleared from the TX buffer.

The Tiger software also supports “9-bit” mode, where each device on a network has an 8-bit binary address, and each byte transmitted has an additional flag bit so the receiver can differentiate between an address byte (starting a message) and data bytes. This is a common protocol used by CPUs such as Z180B, 80C188EB and 8051s.

A series of links allows users to select which of SER0 and SER1 interfaces are used for RS485. (Logic forces SER1 to RS232 mode in PC download mode.)

The RS485 interface hardware can also be used as a TTL-level serial interface. A bias-setting jumper is provided setting a 2.2 volt reference which can be linked via two jumpers to either true or inverted RX-in. The opposite input can then be used for TTL serial, choosing either inverted or non-inverted input. The transmitter provides both true and complement outputs. The links mentioned previously allow both the transmitter and receiver to be permanently enabled, so no TX-control is needed.

A typical application for this is to communicate to a TTL-level GPS system.

RS422 communications can also be provided with this interface. The TX-ON and RX-ON links are inserted and a four-wire RS422 system is then available for long-distance point-to-point communications. (RS422 is always-on differential transmission to a single, remote receiver. RS485 is a multi-drop protocol where multiple transmitters on the line turn on their transmitters when data needs to be transmitted.)

LCD displays and keyboard

Two displays are provided-for with this board. They can be mounted in two ways:

- On the BACK of the board, with spacers from the board to the display in each corner of the display. A separate set of spacers on the four corners of the board to the front panel, behind which this board is mounted, supports the whole assembly. As mentioned above, two displays are possible, a small and a larger one, but both displays use a common data, power, bias and backlight connector. In this mode, all other components and connectors face backwards, away from the front panel;
- From the FRONT (top or component) side of the board, via a flying cable, with the LCD connector on the top of the board as well. In this mode, the board is mounted flat in the bottom or back of the box, and the LCD is mounted separately.

The backlight of the LCD can be turned on or off by the CPU using a special output port bit.

The BIAS of the LCD is set with a trim-pot, and can be jumpered to be a positive bias for normal temperature rated displays, or a negative bias, for wider temperature displays.

The keyboard can also be connected from the BACK of the board, and a 3 by 4 telephone-pad style keyboard is useable via a strip connector with 0.025" square pins at 0.1" spacing. There are sufficient scan pins provided to support a 5 by 4 (20-key) keyboard, but for this, a cable is needed from the keyboard to a connector on the FRONT of the board. This could be a contact switch type keyboard, or a membrane keyboard with a flying tail to this connector.

EEPROM, Powerfail Detector, Watchdog

An X5043 chip provides 512 bytes of non-volatile memory, readable and write-able on a byte by byte basis. It generates a RESETN to the system if it detects Vcc 5 volts has dropped below a threshold, and it also has a programmable watchdog, which is set by software and which then will generate a RESETN pulse if the CSN input is not "tickled" at least once per watchdog timeout period (nominally 1.4 seconds, worst case 1.0 seconds).

Xilinx Gate Array, user I/O

The gate array concept

For many years, JED has used FPGA (Field Programmable Gate Arrays) as the medium for implementing the majority of logic on a CPU board, and this board is no exception.

FPGA technology has a number of advantages for such a system:

- It is downloaded into RAM in the FPGA device (from the CPU FLASH memory) on startup in a couple of seconds, and then provides a wide range of user or JED designed logic as a powerful assistant to the functions provided on the CPU;
- The designs for the FPGA internals are designed on a PC using schematic capture software. After compilation, this produces a binary file ready to incorporate in the FLASH program area as a data file. A simple program loop transfers this into the FPGA;
- Different sizes of FPGA devices are available in the same pinouts, allowing simple and more complex designs to be accommodated on the same PCB. On this board, two devices are possible: The Xilinx Spartan XCS05XL, with 100 CLBs (Configurable Logic Blocks), and 360 flipflops, or the Spartan XCS10XL with 196 CLBs and 616 flip-flops;
- Power consumption is low, typically under 5 mA at 3.3 volts;
- No programming devices, dongles, special cables, etc are needed ... just the serial cable from the PC serial port to SER1 to load a program and a FPGA configuration into the FLASH of the Tiger.

As an example of logic JED has implemented for customers in FPGAs, we have built a variety of counter systems in FPGAs, ranging from multi-axis incremental shaft encoders, stepper motor drivers, 5 frequency counters with time base, etc, and an X10 UART. (On the TIG515, the 1-Wire interface is implemented in the FPGA.)

A 1Mhz ceramic resonator controlled oscillator feeds a global clock into the FPGA, providing a time base for timer-related functions.

Direct digital inputs, 8 bits

A 9-pin connector on the top edge of the board has 8 inputs and a ground, with all 8 signals going into the FPGA, so they can be used just as readable signal inputs read in parallel at an input address, or can go as well into custom logic, such as counters, in the FPGA.

Each input can be pulled up to 5 volts or pulled down to ground by plug-in resistor packs (8 down, 4 up, 4 down or 8 up). Each input then has a larger series resistor for protection from electrostatic pulses or high-voltage connections. Inputs are rated to 36 volts.

The pull-up configuration is intended to be driven by switches or opto-isolators, open-collector NPN transistors or open-drain N-channel FETs (to ground). The pull-down configuration is intended for voltage sources, eg switches or PNP transistors driven from a positive voltage source.

Multiplexed analog/digital inputs, 8 channels

Eight inputs (and ground) on the lower edge of the board are provided. The eight inputs are configured by a array of 8 rows of 7-pin sockets in a 0.1" spaced matrix. The output of this matrix feeds an 8-input 4051 analog/digital multiplexer. In this matrix, users can insert various resistors or filter capacitors.

The first three rows of holes allow for pullup resistors to 5 volts or load resistors/pull-downs to ground. These could be 200 Ohm, used for 4-20 mA analog loop loads, or 1K ohm loads for temperature sensors. The pullup resistors can be part of a resistance sensing circuit or current source for a thermistor. If it is a digital signal being sensed, the pullup or pulldown resistor allows contact closures to ground or switched voltage inputs to be sensed.

The next two rows of holes hold a series resistor for each channel. This can be just for protection, or can be part of a voltage divider or filter pair. Normal value is 10K ohm.

The last two rows of holes include ground, allowing the second resistor of a voltage divider or a filtering capacitor to ground to be installed.

The multiplexer is addressed by an OUT instruction to a latch in the FPGA. The output of the multiplexer is buffered with a Rail-to-Rail Op-amp, and connects to a four-way link. This signal can be connected to an E-Tiger analog/digital input channel to be sensed with an input instruction, or read as an analog input with a 10-bit Analog to Digital conversion. (The Vcc rail is the voltage reference for this conversion, so calibration of the Vcc by saving a scale factor number in an EEPROM location might be advisable for best accuracy.) The buffered signal can also be connected to a high-accuracy 12-bit converter.

Optional 8-channel, 12-bit Analog to Digital converter

A MAX189 serial Analog to Digital converter allows for higher accuracy conversions than the E-Tiger 10-bit system. This ADC has a very accurate, temperature compensated, trimmed reference at 4.096 volts (giving a conversion of 1 mV per bit, or 4,000 counts for 4 volts input.)

Modular input/output system

At the far end of the board are two TIG525-family expansion module connectors. These allow a range of plug-on peripherals to be added to the board, including 16 channels of FET outputs, 16

channels of digital inputs, a variety of SPI-connected interfaces, including Digital to Analog converters, microprocessor based counters, etc.

As a default, the board is normally provided with 8 MTD3055 power FETs on the lower four channels of the two modular systems. These FETs are protected by catch diodes at a 60-volt rating.

Analog input functions, eg chopper-stabilised signal amplifiers, buffers and multiplexers can occupy these modules, and can feed a common “analog bus” to the jumper, to also feed either the E-Tiger 10-bit ADC or the 12-bit system. (If the 12-bit system is connected to the modules, the 8-way multiplexer can still connect to the E-Tiger ADC/IN pin, so these 8 inputs are not wasted.)

(These modules are also used on the JED TIG520 and AVR590 boards.)

DIP-Switch input system

An 8-way DIP switch is able to be read by the CPU via a shift register. It can be read using the SPI interface. This could be used, for example, to set an address in a multi-drop RS485 network system. (If a user wanted to provide 8 extra inputs to the board, the switch could be replaced with an input connector to sense 8 external contact closures, relays or push-buttons).

Dallas/Maxim 1-Wire interface

A three-screw terminal interface is provided for interfaces to Dallas 1-wire systems, along with a 5-volt Vcc connection to external devices. This interface uses logic in the FPGA to generate timing for the 1-Wire interface, with counters generating timing for “0” and “1” bit writing, the RESET pulse, and the sample time for reading. These are controlled by the 1Mhz clock. 1-Wire devices are covered extensively in Dallas/Maxim’s www site, but in summary, they allow distributed I/O devices and temperature sensors and thermostats in small packages to be parallel connected across a wire run and addressed via a laser-written unique code. The availability of 5 volts allows devices which need extra power to be supported.

A P-FET from 5 volts to the centre (1-Wire) pin can be used as a switched 5 volt output (if no 1-Wire functions are needed), or as a boost during temperature conversions for a DS1820 family device.

Optional Real Time Clock

A Dallas/Maxim DS1305 Real Time Clock is powered by a lithium battery, and provides clock and calendar information to the CPU via a serial SPI interface using the E-Tiger SHIFT instructions.

The RTC also has an alarm function allowing the user program to set up a future alarm time, and the power the board down. When the set alarm equals the current time, the power is turned on again, and the board starts execution. When the power switching option is installed, a three pin power input socket is installed, with one pin for unswitched (always on) and one pin for switched input power.

Ninety-six bytes of non-volatile battery backed RAM are also provided in the RTC chip, accessible via simple SHIFT instructions to READ and WRITE bytes. This can be used to hold pointers to FLASH memory addresses.

MMC/SPI FLASH memory expansion

An 8-pin connector allows for a plug in expansion or MMC FLASH card expansion for an SPI interfaced FLASH card or plug-in module. This is a common pinout to one developed by JED, and used on the TIG505 board. Up to 32M bits of Atmel DataFLASH memory can plug into this connector.

Power Supply System

A low-drop-out linear 5 volt regulator powers the TIG515, and 5 volt power is available to external systems via the 3-pin 1-Wire connector, switched if necessary. A P-channel FET controls the power from the RTC alarm if desired.

The input range is as low as 5.5 volts in to 18 volts. The regulator is an “automotive” type from National, with +/-60 volt “load dump” transient protection (not with the FET switch). Thus the board will work form 6 volt Gell cells or 12 volt automotive power.