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The BASIC Tiger and Tiny Tiger microprocessor modules from Wilke (Germany) present an easy way for builders of embedded control systems to build, program and put small systems into production. The modules are available in a range of memory capacities: Tiny Tigers can have 128kB/32kB, 128kB/128kB, 512kB/512kB or 2MB/512kB respectively of FLASH and RAM.

This board uses the Tiny Tiger module and places it on an 116mm by 101mm board to make it easy for scientists and engineers to use the Tiny Tiger for small systems without having to design a printed circuit board. The board has a Xilinx XC5202 gate array and input protection or FET drivers between the Tiger and all the I/O screw terminals, isolating the Tiger from the outside world for ESD and EMC purposes. Tiger pins are bypassed to a grounded PCB plane, and all supply rails and Tiger pins are EMC filtered.

(JED also makes a larger Tiny Tiger board, the TIG505, for users who need more I/O, larger gate array, larger keyboards and extra interfaces.)

The Xilinx can be reprogrammed by users downloading a data file from the FLASH, so users can re-wire the system between the pins and the Tiger, adding their own counters, pulse generators, shift-register filters, etc.

Users of this board have 12 digital input terminals, 4 analog input terminals, 13 outputs with open-drain FETs, and a switched 5 volt output. There are two serial ports for communication. One of these ports can be used with an optional opto-isolated RS485 interface.

This board can be used as a conventional single-board-computer, or can have a 4-line by 20 character LCD added on top, with a five-key set of push-buttons (or a small XY keyboard) for "menu" style operator set ups, etc.

The Tiger concept and EMC.

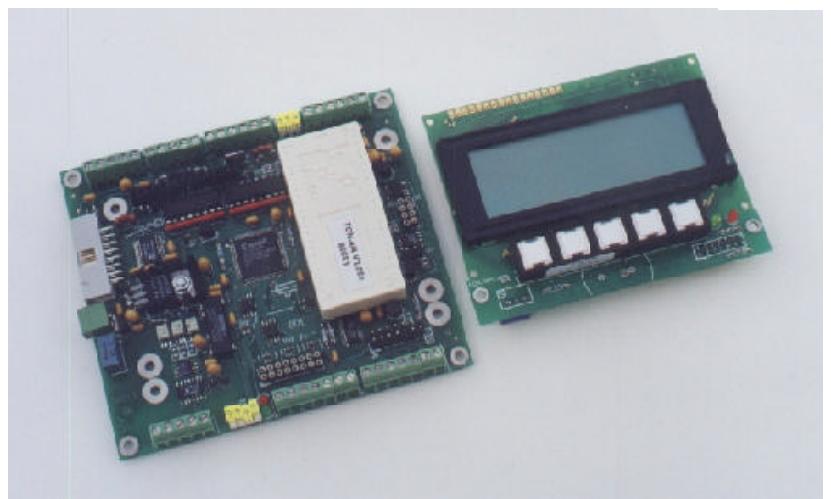
The BASIC and Tiny Tigers are small, 20 Mhz clock microprocessor modules with the high speed bus and memory system housed in a plastic housing, ready to use in applications without users having to worry about the intricacies of high speed bus timing, decoding or paging and addressing. The interfaces necessary for a standard small microprocessor system, (dual UARTs, a complex counter-timer system, plenty of memory (FLASH and CMOS, battery-backed RAM), Real-Time-Clock and a ten-bit four channel analog input system) are all housed in the module.

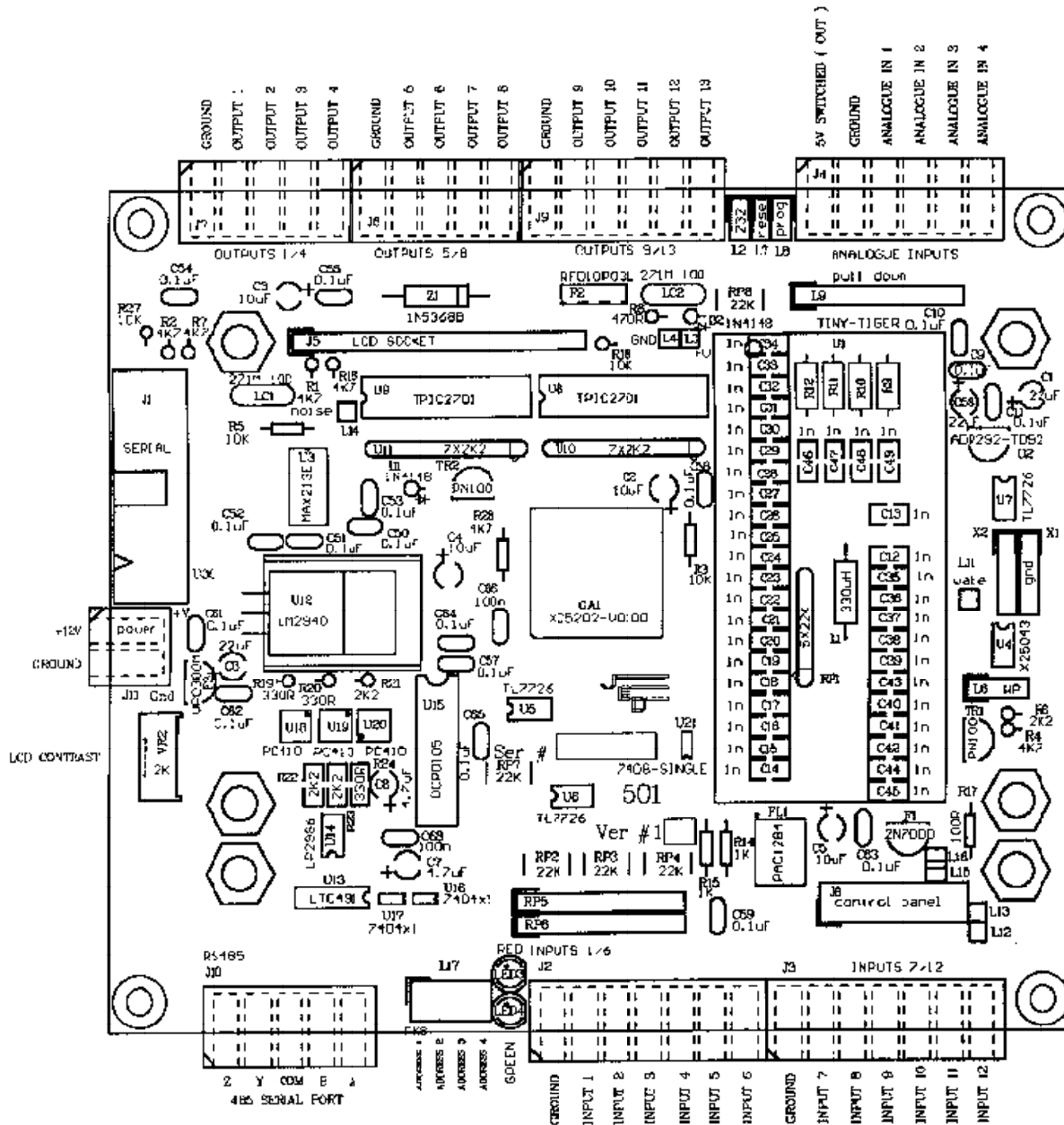


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TIG501, Tiny Tiger controller board for small embedded control applications.

- Uses Tiny Tiger from Wilke Technology (Germany), and allows high-performance systems to be developed at low cost, direct from a PC;
- Low power: board draws approx. 100 mA;
- BASIC multitasking allows modular development of programs with controlled interaction between segments. (Up to 32 tasks allowed);
- Powerful development system runs under Windows, edits, downloads to FLASH and remotely debugs target at source level;
- JED board made in Australia to support the Tiger allows "screwdriver" building of systems, with gate-array reprogrammability of hardware in a Xilinx gate array;
- Xilinx provides Dallas iButton support via hardware timing generator; and
- Opto-isolated RS485 interface for local area serial networking (optional).





Because all the high-speed buses occupy a small volume, RF radiation is very much reduced over a system where the buses occupy a large PCB surface area acting as an antenna. All I/O lines from the Tiger are bypassed to the ground plane on the back of this board, so any RF which escapes via device pins is bypassed before it can radiate. Supply lines are also L-C filtered.

Memory system and download mode.

The TIG501 board can have a choice of any of the four different Tiny Tigers installed, with RAM from 32kB to 512kB and FLASH from 128kB to 2 MB.

The choice obviously depends on program size, but users should be aware that if an LCD display is used, the complex device drivers provided only allow about 10 kB of RAM for user data, and so most applications, except for very price-sensitive projects, would be well advised to use at least the TCN-1/1 (128kB/128kB).

Download to the FLASH occurs when the compiler program (running on the PC connected to a serial port) detects a download request. The Tiger must have the PC jumper switch set to "PC mode" as RESET is triggered.

Xilinx gate array and options it provides.

A Xilinx XC5202 gate array in a 100 pin package provides the TIG501 system with 81 I/O lines and 64 Configurable Logic Blocks, (with four flip-flops and function generators each). It is a low-power, RAM-based gate array, so after power-up or reset it is necessary for the Tiger to run a small program to load the configuration bit map into the Xilinx. The file is loaded into the FLASH by a DATA statement in the program at compile time, and the Xilinx loader program reads it from there and loads the Xilinx. (This takes about a second).

There is sufficient space in this device for quite a lot of logic: it can be designed on a screen using schematic entry software and routed using the Foundation low-cost development package from Xilinx. The advantage of such a

configurable hardware system is the one PCB and I/O system can have its hardware completely redesigned or altered in quite simple ways. Also, once the board or control system has been tested for EMC with a worst-case design, alterations in the gate array need no certification.

Input system, on 14 screw terminals.

Across the top of the lower edge of the TIG501 board are twelve general-purpose input connectors (and two ground screw terminals). Input lines can be pulled up to Vcc or down to ground with a resistor array, usually 4k7. A series resistor connects the input pin to the gate array, with a 7726 active clamp on the line to Vcc and Ground, so that the gate array is not damaged by excess voltages or electrostatic pulses to the pin. Input voltage ranges can range + to - 24 volts continuously but can withstand much larger ESD transients. The threshold is at TTL levels.

This input arrangement allows users to select between a voltage input mode (pull-down resistor to ground), or contact or opto-isolator mode (pullup resistor to Vcc).

The standard JED gate array provides these inputs to readable ports implemented in the gate array at addresses 80 and 81 (hex).

Considerable power is provided in the Xilinx gate array. Many flip-flops are available to build logic between the input pins and the registers read by the Tiger IN instruction.

The PLSOUT instruction in the Tiger (Port P86) is routed on the board to a global clock on the Xilinx, and so can be used to generate time bases for counters and timers implemented in the gate array. This is programmable over a wide range of frequencies: typically it is set to 500 kHz.

Output ports, on 17 screw terminals.

The outputs consist of 13 N-channel power FETs with the sources grounded and the drains connected to the terminals. Each output has a fly wheel catch-diode to a zener to 47 volts. The drivers are TPIC2701s, with a pull-down resistor on the gate of each FET to ensure it is OFF with the gate array uninitialised on RE SET.

A 14th output is a P-channel power-FET with drain to Vcc, providing a switched 5 volt rail output (to power sensors, etc.)

The standard gate array allows the FETs to be driven 8-bits in parallel, at addresses 10 and 11 (hex) using the OUT instructions, which include masks allowing individual bits or groups of bits to be addressed without affecting others in the same port. Users can add their own driving logic in the Xilinx gate array. This can include counter and pulse generation logic, to, for example, drive stepper motors.

Serial ports, RS232 and (optional) RS485.

A 16-pin connector at the left-hand side of the TIG501 has its first 9 pins allocated for SERIAL-0 RS232 port, wired as a DE (i.e. the same as a PC would pig nut to a D9 connector.) A null-modem cable is necessary to connect this port to a PC, but it can connect to a modem (D9 or D25

via an adaptor) directly. The Tiger supports CTS/RTS handshake with the SERIAL-0 driver, but the other RS232 lines terminate in ports in the Xilinx and are readable or settable by IN or OUT instructions.

SERIAL-1 RS232 has three wires (TX, RX and Gnd) on the same connector, and this connects to the PC for download. Download mode from the PC is selected by the PC/RUN switch.

An optional RS485 full duplex (4-wire) or half-duplex (2-wire) can be factory-installed on the TIG501 if it is intended to use the board in multi-drop distributed RS485 networks. The interface is fully opto-isolated, and the TX "connect-to-line" function is provided in the Xilinx with a hardware timer.

A 5-pin screw terminal connects to the RS485 lines. Switchable terminations are available on both RX and TX lines, and biasing resistors are provided on the RX line as well (when the RX termination is switched in.)

(If two RS485 ports are needed in a system, or if SERIAL-0 is in use for some other purpose, JED makes RS232 to RS485 converters in 25mm by 50mm by 100mm cases which plug into the SERIAL-0 cable directly.)

Other serial interfaces: I²C

On the same connector used for the two RS232 channels are four more pins allocated for I²C use.

- SCL, the I²C system clock; and
- SDA, the I²C system data.

I²C operations use a driver supplied by Wilke which sets port addresses on the Tiger for data-in, data-out and I²C clock, and the handbook suggests using a diode in series with the data-out pin to simulate the I²C open collector drive. In the TIG501, we route the selected I²C clock port pin to the SCL pin, and the data-in and data-out pins are combined onto a bi-directional pin on the Xilinx by programming an I/O pin as an open-drain output with simultaneous input, and this is the SDA pin. (Bits in a Xilinx control register sets up these SCL/SDA pins.)

The I²C lines have 4K7 pullups.

Because the I2C communications are generated by a CPU under software, rather than from hardware registers, the Tiger can be the only "Master" in a system, driving "Slave" peripherals. This can include other microprocessors with Slave mode support, e.g. some of the Philips 8051 family equipped with hardware register I2C support can be initialised as "Slave" only I2C devices.

Note: two Tigers cannot talk to each other via I²C, as they are both masters.

Other serial interfaces: Dallas 1-wire

Inside the Xilinx gate array is logic to generate the appropriate timed pulse generation and sample timing for signal sensing to support Dallas "1-Wire" interfaces. The switched 5-volt output port provide the low-impedance Vcc drive for supporting multiple temperature transducers (e.g. the Dallas DS1802) along a "1-wire" network. (It really is two wires: a ground wire and a signal/power sup-

ply line, but Dallas insist this is only “1-wire”. We will humour them!) To use the one-wire functions in the Xilinx, it is necessary to link an output port pin and an input port pin on the screw terminal connectors. Multiplexers allow one, two or four terminal pairs to be used for 1-wire runs, allowing each run to be used for different purposes...e.g. one for a multi-sensor temperature monitoring run, one for remote I/O ports and a couple for identification buttons.

The combination of the Dallas interface and the optoisolated RS485 makes the TIG501 an ideal board for distributing around a factory, building, winery, controlled-atmosphere fruit shed or similar installation, where data can be gathered by a combination of analog and digital means and processed locally or communicated back to a SCADA or PC control site.

Dallas has information about “1-Wire” systems and concepts at: www.dalsemi.com (“1-Wire” is a trade mark of Dallas Semiconductor.)

Watch-dog timer and RESET generator.

A Xilinx X25045 multifunction chip generates a “RESET” to the Tiger and initialises the Xilinx ready for a configuration load on initial power up, and whenever it detects the Vcc dropping below a 4.5 volt threshold.

This device contains 512 bytes of EEPROM, which can be used to hold any user-defined data. A section of the EEPROM can be hardware write-protected (with a jumper) after programming, containing, for example, calibration data. The device is read and writes using serial functions in the Tiger. Non-volatile registers in this device control the watch-dog timer function, and the user program must “tickle” the device before time-out, otherwise a system reset will be generated. The time-out time is user-settable in an internal non-volatile register, but external hardware on the TIG501 disables the watch-dog during PC to FLASH program download, so that time-outs do not interrupt PC-controlled debug operations such as single stepping and breakpointing.

LCD display for text or pseudo-graphics.

Wilke have provided very extensive LCD support in the Tiger, and this is supported by a connector for a 4-line by 20 text display. The software drivers provide user-writable character sets, so pseudo-graphics, bar graphs, etc. can also be displayed.

Keyboard scan and five-key keyboard

The Xilinx gate array provides the logic to match the decoder and scanner system Wilke keyboard scanning software requires...a column of the keyboard is scanned at 1 millisecond intervals, and debounced by the driver. Users can define the ASCII code corresponding to each key coordinate, as well as defining control and shift functions or auto-repeat mapping.

A 4 by 5 matrix keyboard scan is provided on connector J6, along with other control panel functions, such as a beeper drive and the status LEDs and LCD display contrast bias control. A 14-pin IDC connector take the keyboard scan across to an external keyboard.

A small PCB, **TIG501KB5**, is available to mount just below the LCD display with five user-legendable 12mm square keys from Greyhill. This small keyboard is intended for use as a menuing system, with keys used to select between menu items, and a couple of keys allocated for increment/decrement of selected menu items, e.g. setting times, dates or process variables and setpoints.

Analog inputs: 4 channels, 10 bits.

The Tiger has a built-in analog to digital converter, and an external reference, and has a 0 to 4.096 volt range.

A set of four, two-pin socket strips allow users to install their own load resistors (L9) or voltage dividers for wider input ranges (X1, X2), as well as adding filtering of noisy analog sources. A series 10 Kohm resistor is installed, and in conjunction with a 7726 clamper, the input of the Tiger is protected against ESD and 48 volt steady-state signals.

If a 200 ohm load resistor is plugged into the pull-down connector, a 4-20 mA current feeds a 4 volt maximum into an analog input channel.

Assorted other I/O from the Xilinx.

Several other I/O functions originate in the gate array:

- A tone generator with loud speaker driver, able to generate “key-clicks” “beeps” and “alarms” of controllable length and frequency (using a programmable counter in the Xilinx);
- Two LEDs (red and green) which can mount on the TIG501 PCB (half way along the lower connector strip) or on either the 5-key keyboard or a remotely mounted user-supplied keyboard (the red LED is ON during Xilinx configuration load, and goes OFF when load is successful);
- 5 volt switched “sensor” power to a screw terminal.
- Four switch inputs from a switch along the lower edge of the pcb allow users to enter a 4-bit number for program option selection, or if the RS485 serial multiplexer interface is being used, these switches can select one of 16 node addresses.

Battery power for Real-Time-Clock

The 128kB and 512kB Tiger modules include CMOS battery-backed RAM and a seconds-counting Real-Time-Clock. A rechargeable 160 mAH NiMH battery is charged on the board by a resistor-diode combination. This battery is normally mounted by gluing it above the gate array and wiring it to the PCB.

Automatic switching to battery backup is provided inside the Tiger module, but this board does not have system power switching controlled by the clock. The alarm pin from the Tiger (an open-drain output) is available on a pad if users wish to add Tiger alarm-output controlled power switching. (Note: the TIG505 does incorporate such circuitry.)

Power regulator.

Screw terminals at the left of the PCB, and a five volt regulator allow the TIG501 to run from an external 6 to 12 volt power source. Power consumption is 100 mA.